FIG. 1 (a)

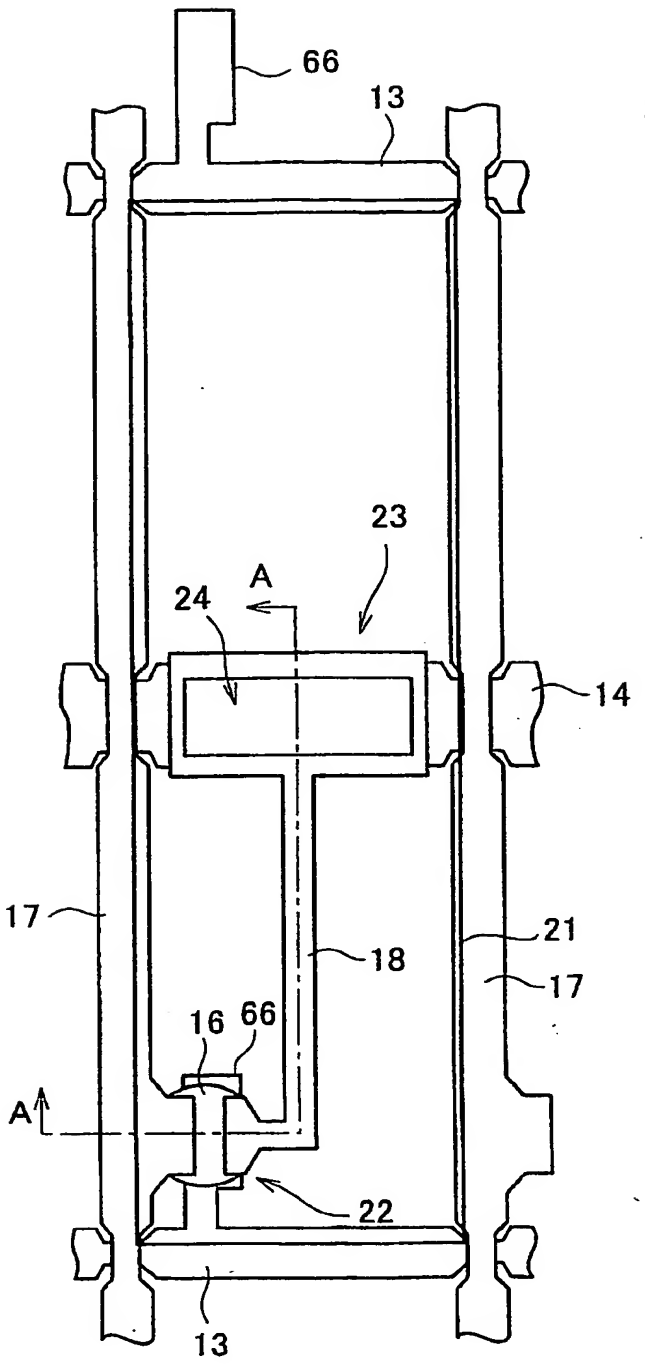
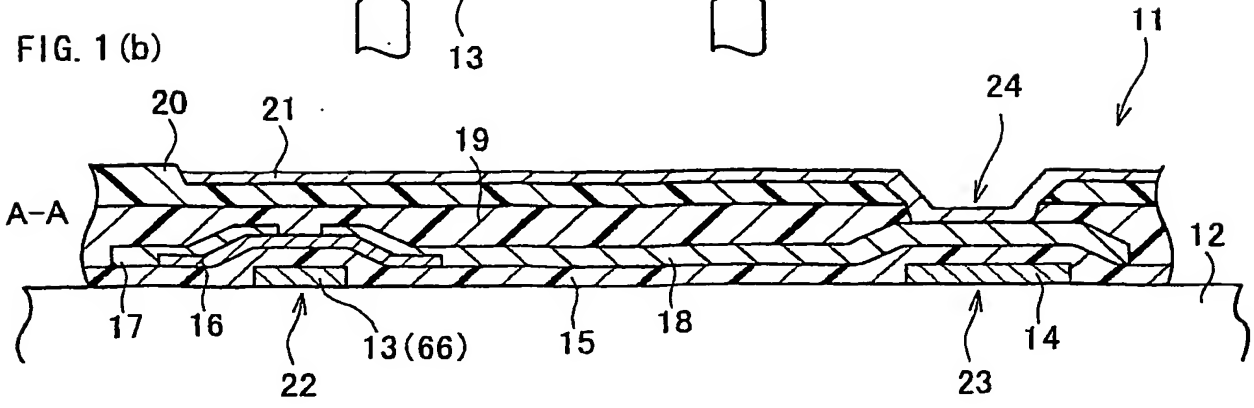

66
13
11
23
A
24
14
17
18
21
17
16
66
A
22
13

FIG. 1 (b)


11
20
21
19
24
A-A
12
17
16
22
13(66)
15
18
23
14

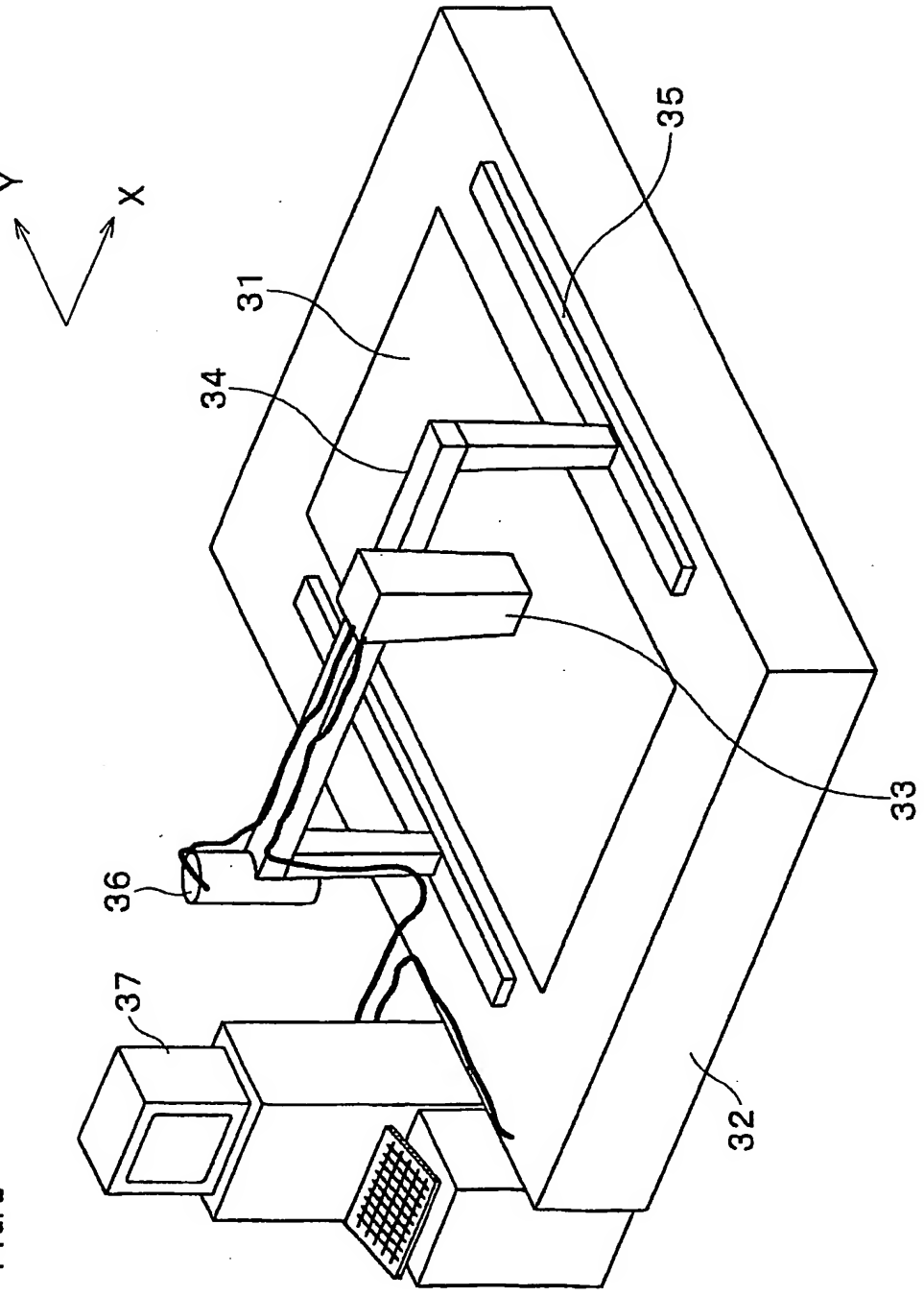


FIG. 2

FIG. 3

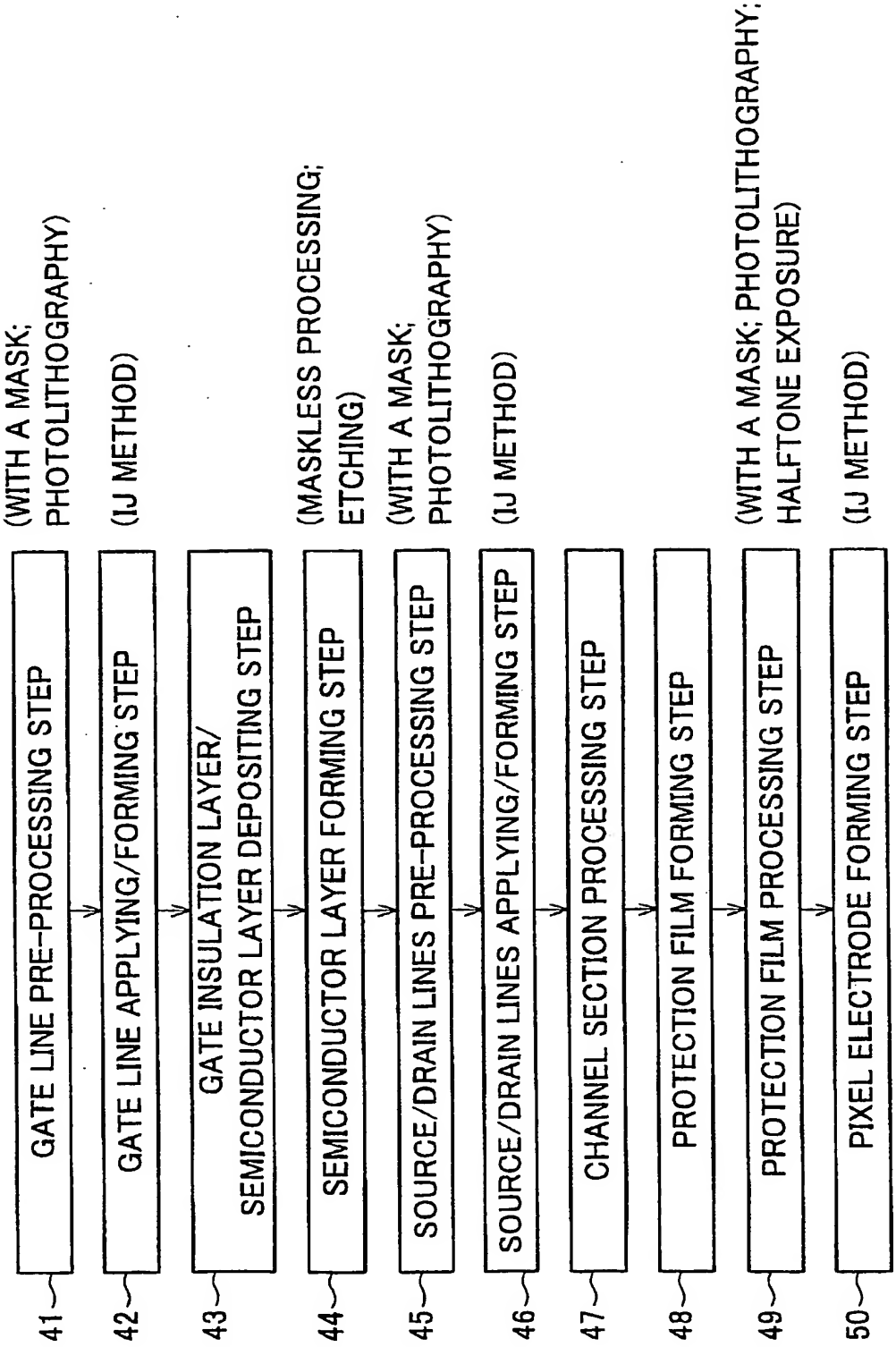

41
GATE LINE PRE-PROCESSING STEP
(WITH A MASK; PHOTOLITHOGRAPHY)
42
GATE LINE APPLYING/FORMING STEP
(IJ METHOD)
43
GATE INSULATION LAYER/ SEMICONDUCTOR LAYER DEPOSITING STEP
44
SEMICONDUCTOR LAYER FORMING STEP
(MASKLESS PROCESSING; ETCHING)
45
SOURCE/DRAIN LINES PRE-PROCESSING STEP
(WITH A MASK; PHOTOLITHOGRAPHY)
46
SOURCE/DRAIN LINES APPLYING/FORMING STEP
(IJ METHOD)
47
CHANNEL SECTION PROCESSING STEP
48
PROTECTION FILM FORMING STEP
49
PROTECTION FILM PROCESSING STEP
(WITH A MASK; PHOTOLITHOGRAPHY; HALFTONE EXPOSURE)
50
PIXEL ELECTRODE FORMING STEP
(IJ METHOD)

FIG. 4(a) (GATE LINE PRE-PROCESSING STEP)

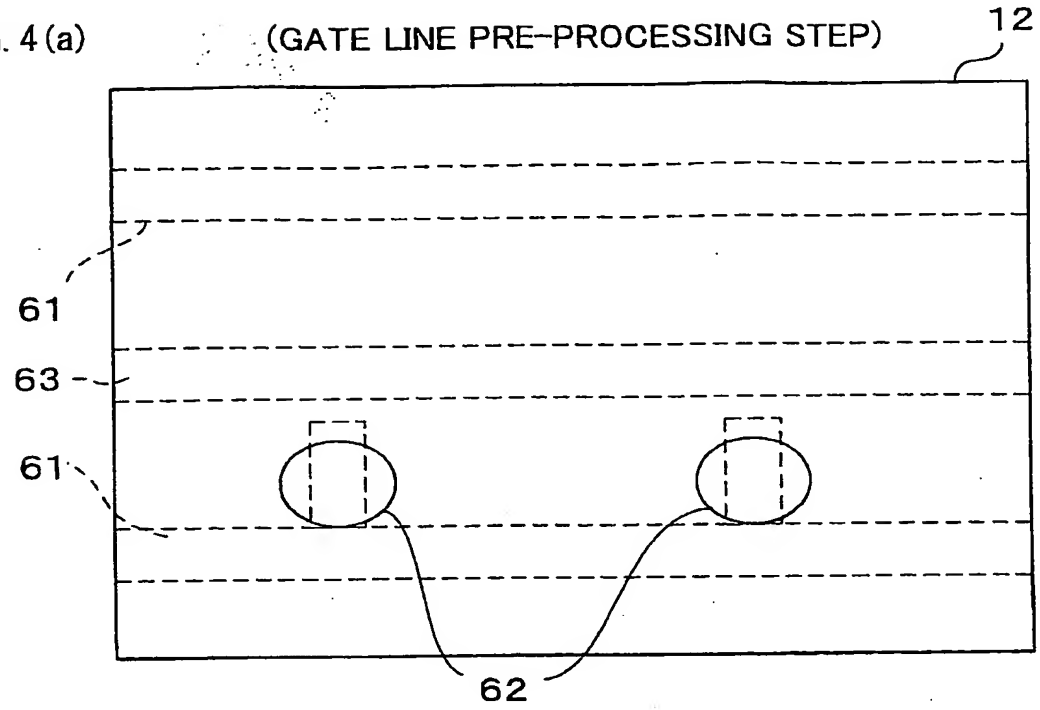


FIG. 4(b) (GATE LINE APPLYING/FORMING STEP)

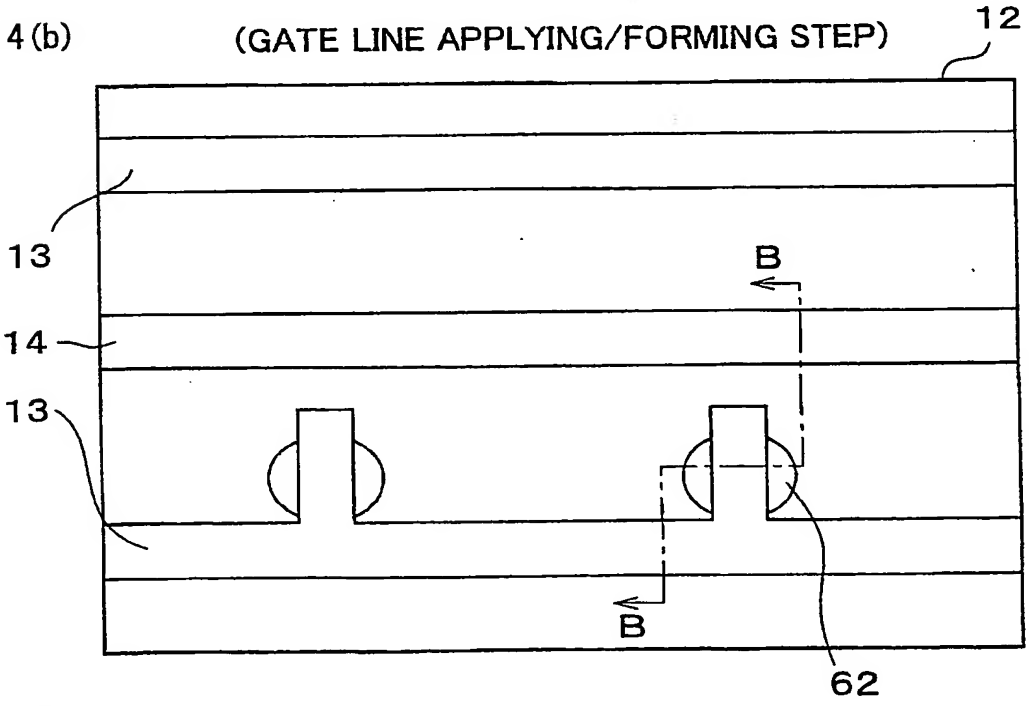
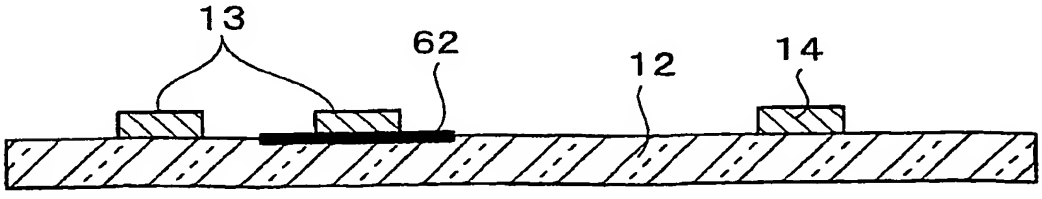


FIG. 4(c)



(B-B CROSS-SECTION)

FIG. 5(a) (SEMICONDUCTOR FORMING STEP)

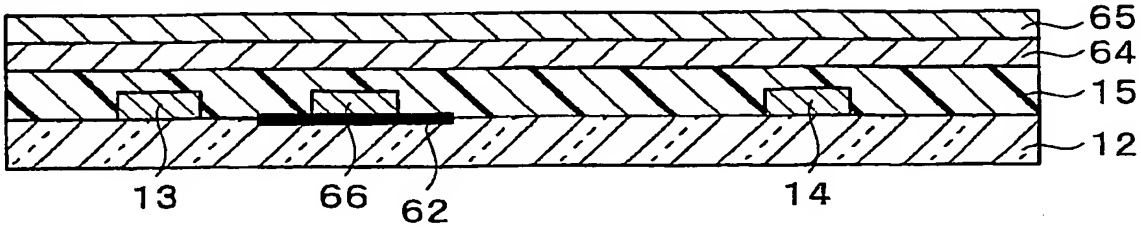


FIG. 5(b)

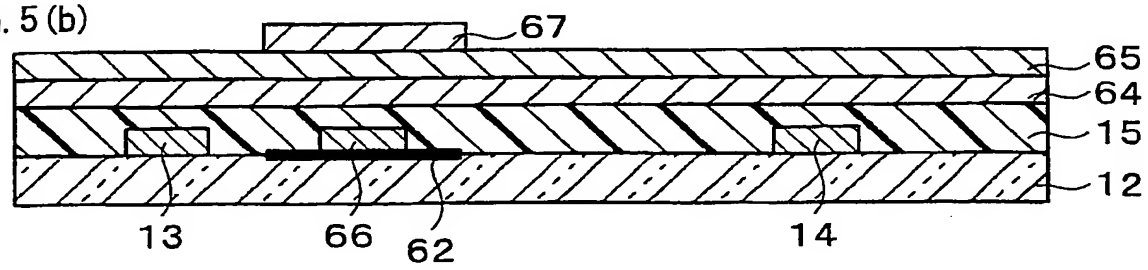


FIG. 5(c)

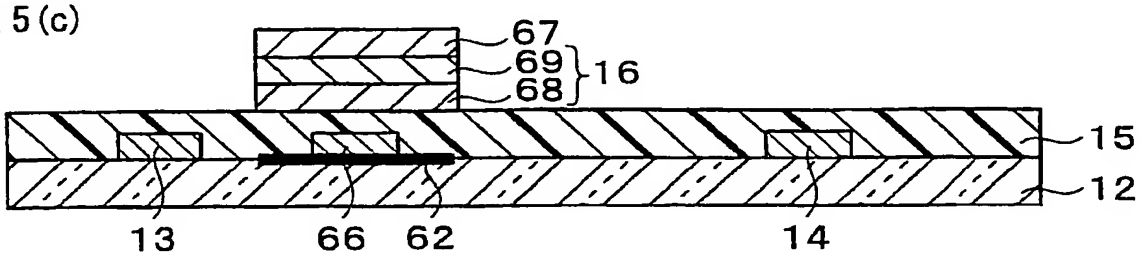
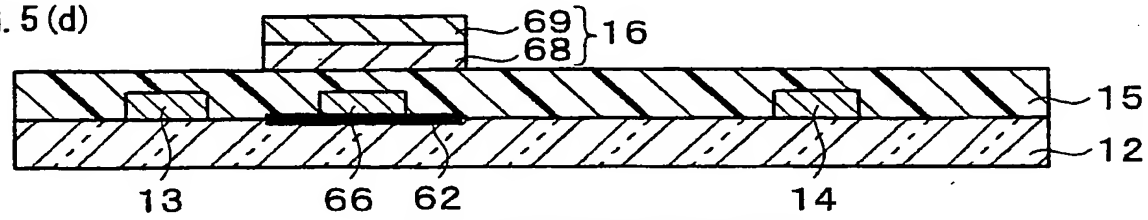


FIG. 5(d)



(C-C CROSS-SECTION)

FIG. 5(e)

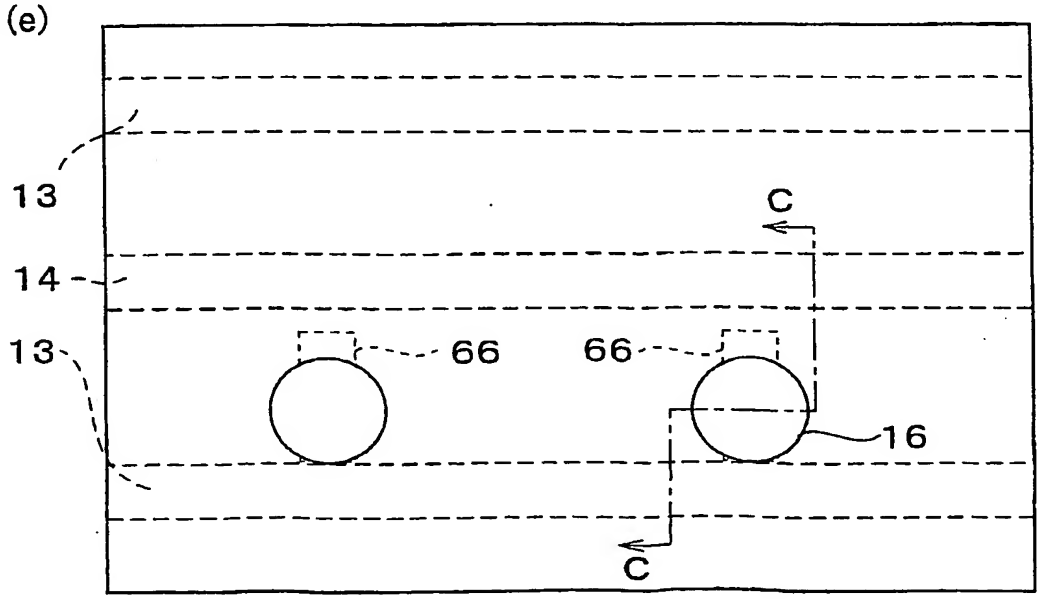


FIG. 6(a) (SOURCE/DRAIN LINES PRE-PROCESSING STEP)

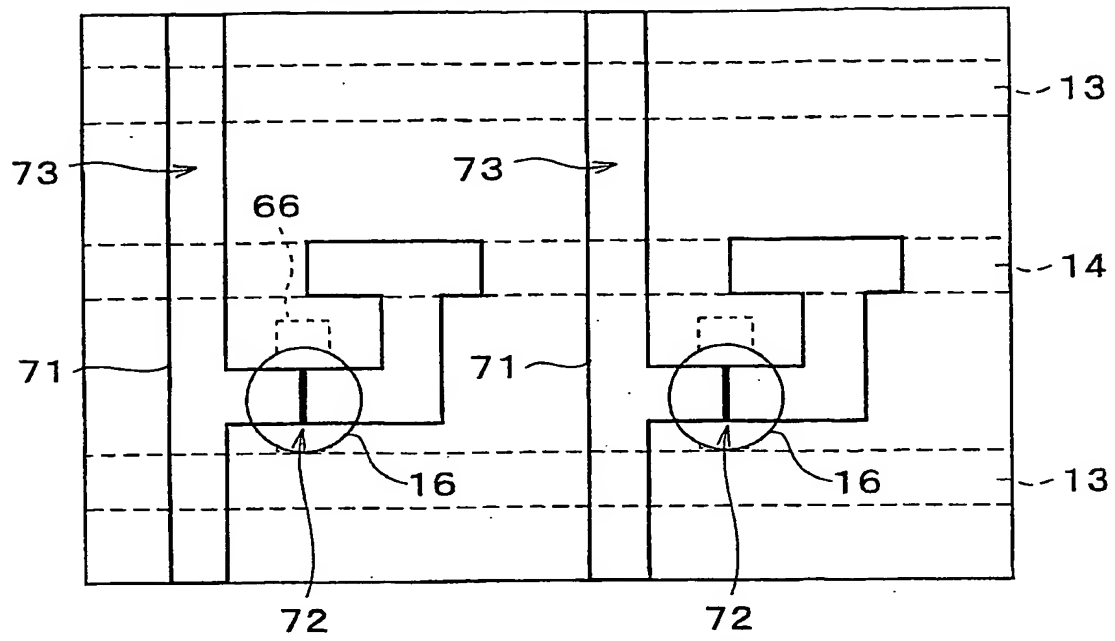


FIG. 6(b) (SOURCE/DRAIN LINES APPLYING/FORMING STEP)

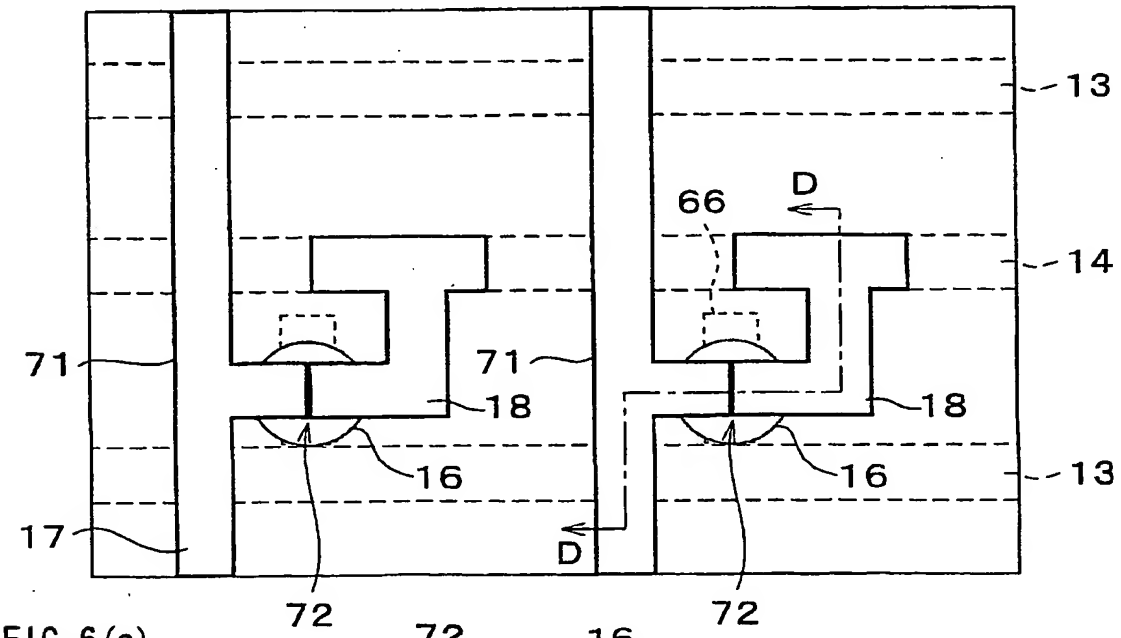
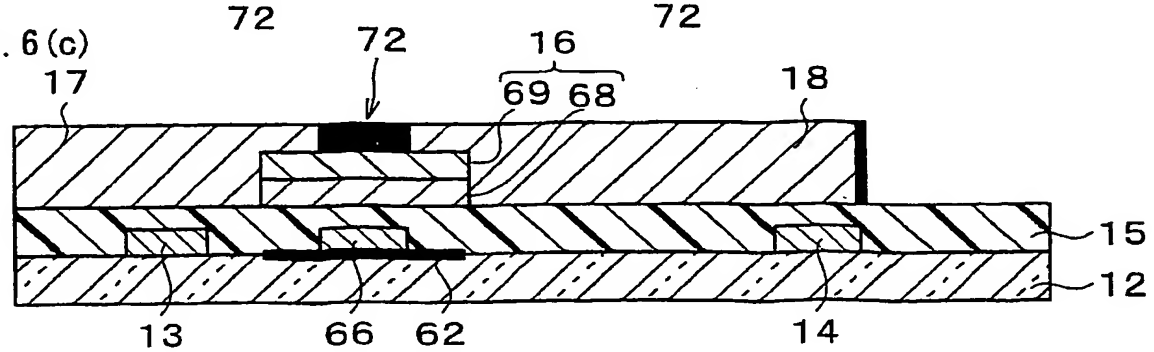


FIG. 6(c)



(D-D CROSS-SECTION)

FIG. 7

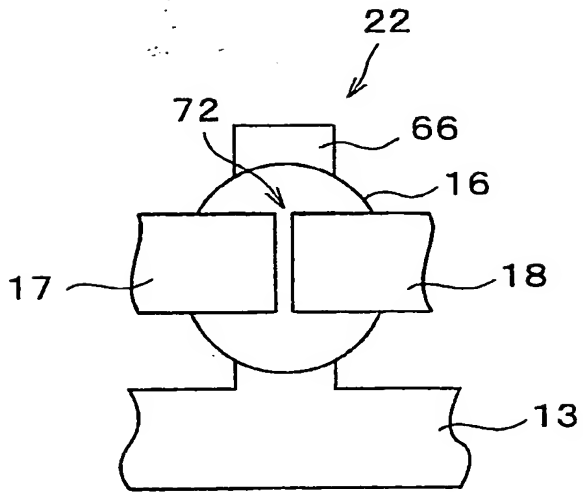


FIG. 8(a)

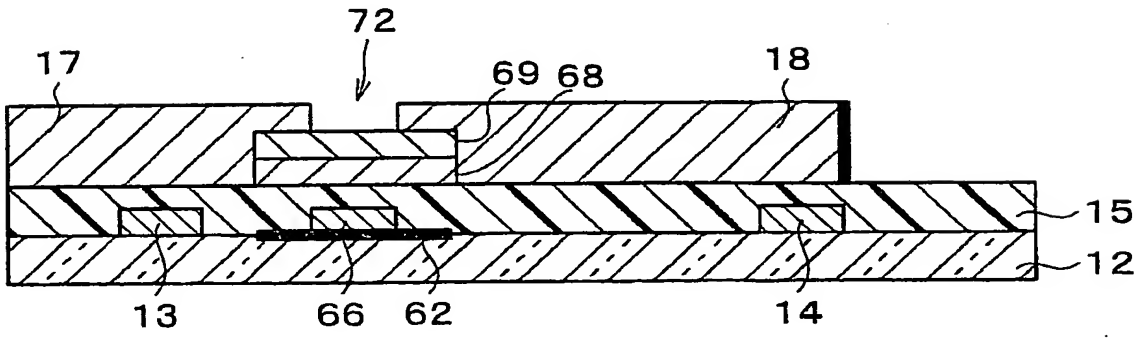


FIG. 8(b)

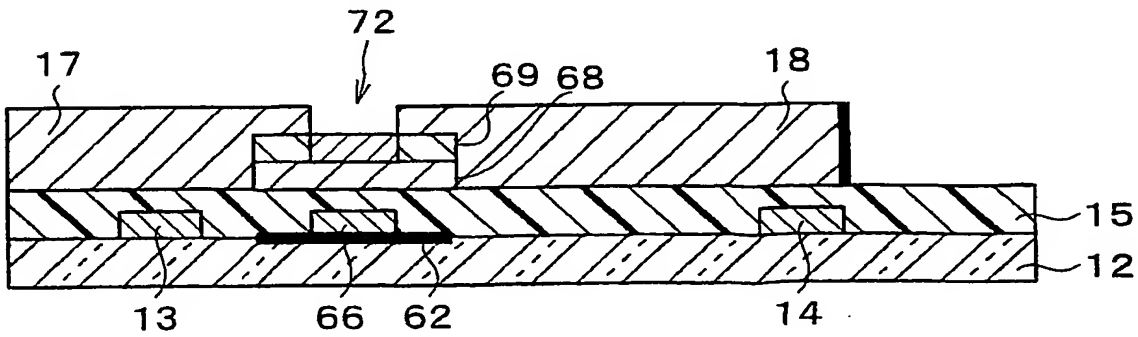


FIG. 9(a)

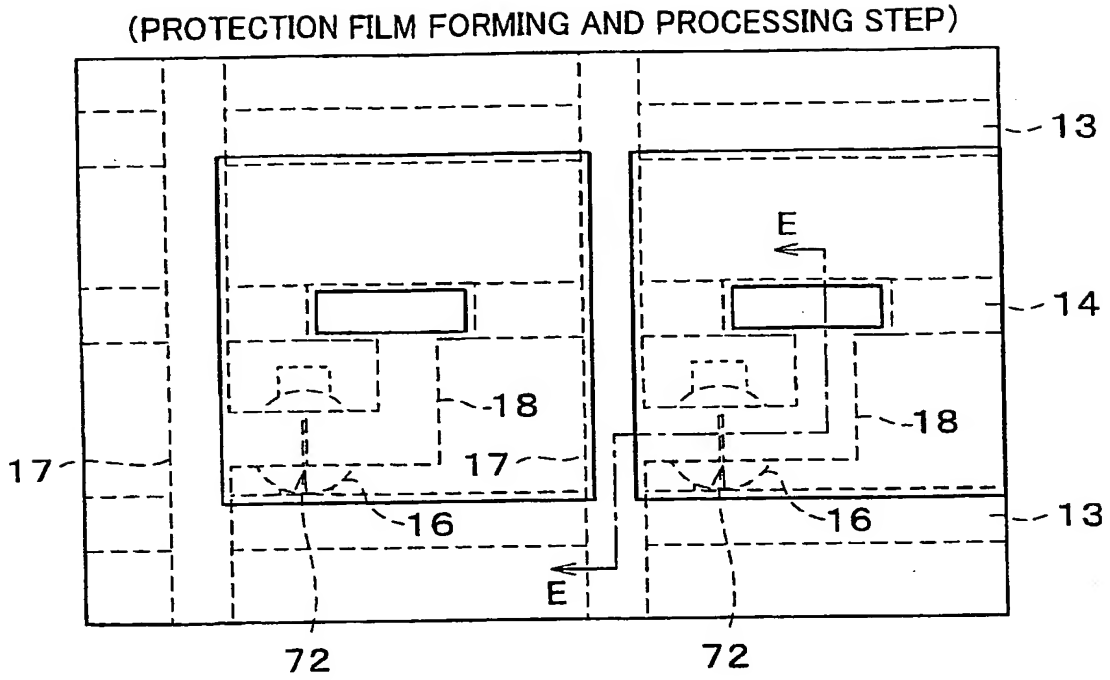
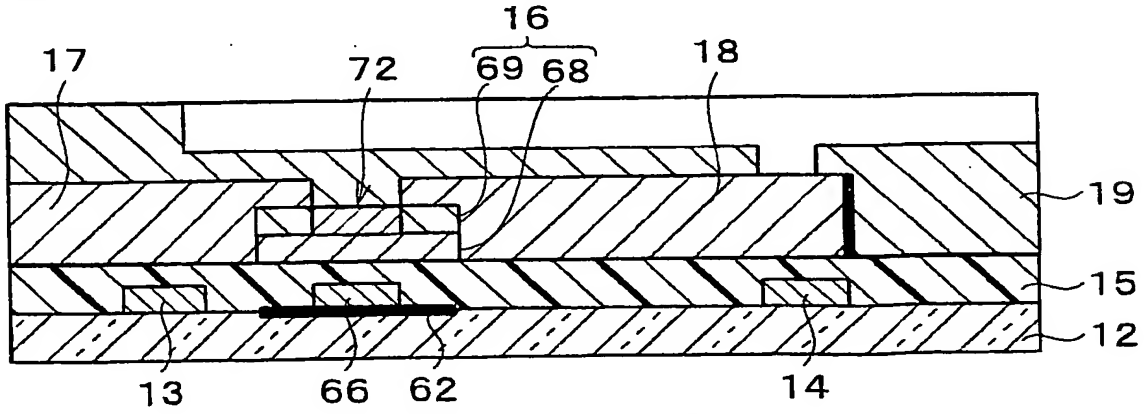


FIG. 9(b)



(E-E CROSS-SECTION)

FIG. 10(a)

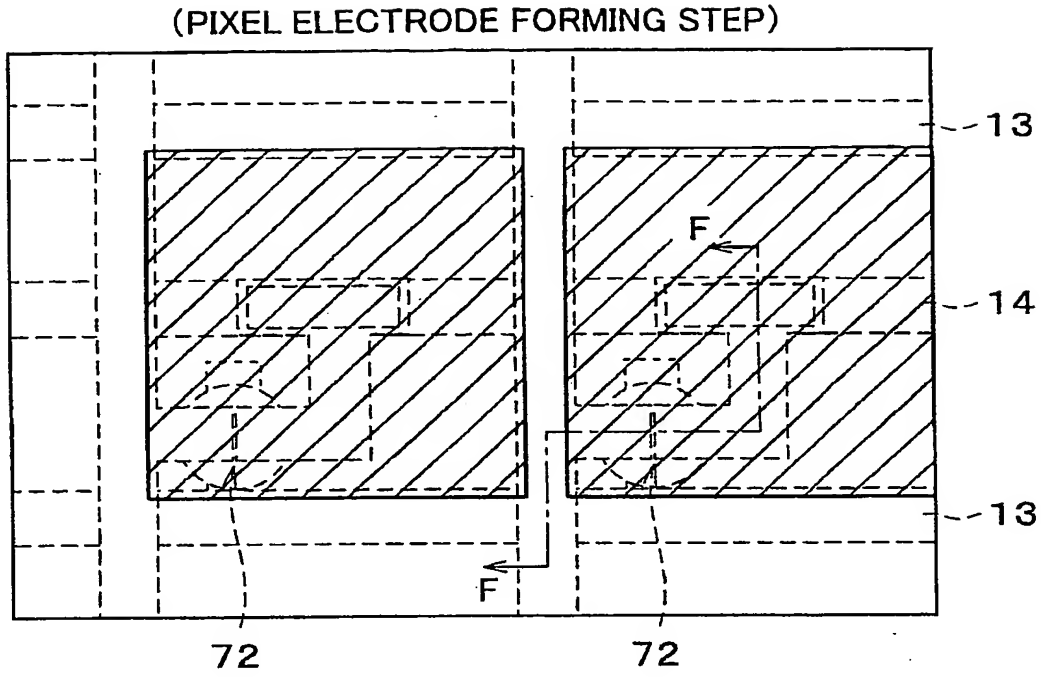


FIG. 10(b)

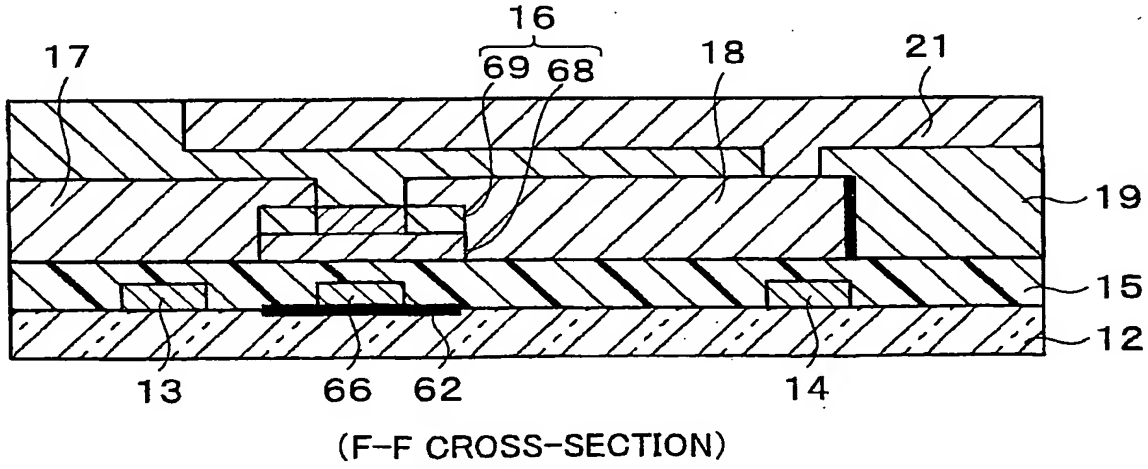


FIG. 11 (a)

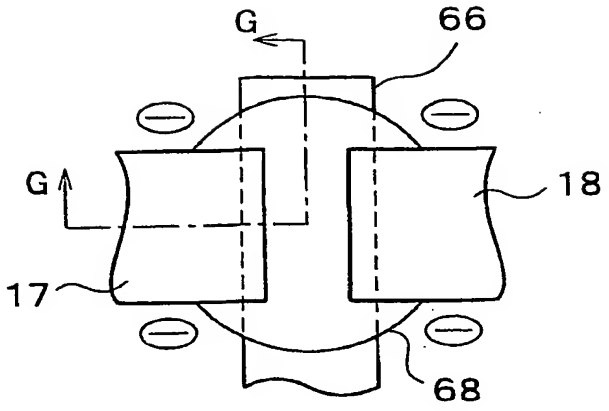
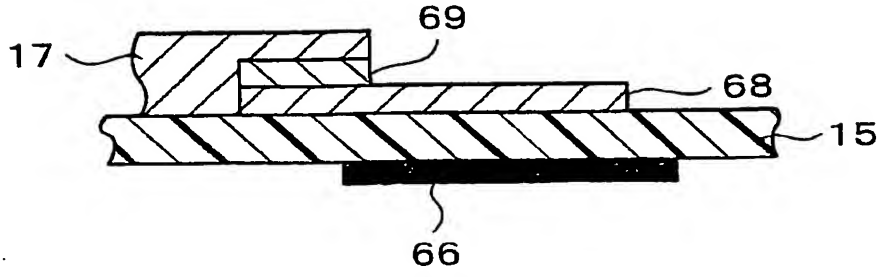


FIG. 11 (b)



(G-G CROSS-SECTION)

FIG. 12(a)

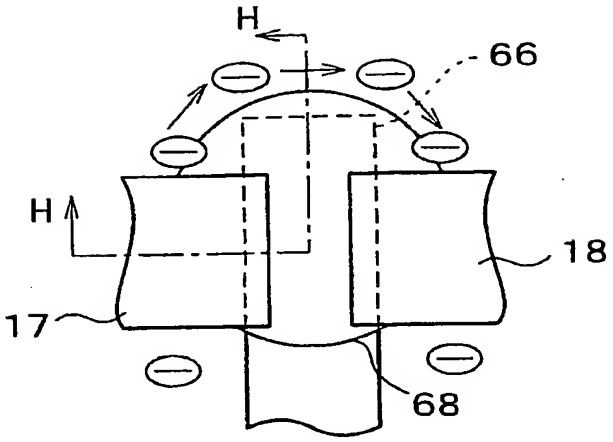
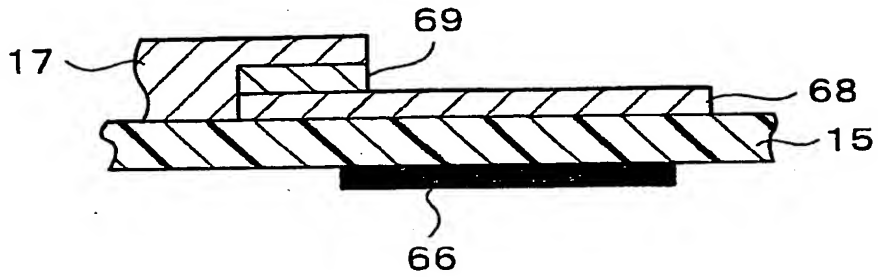


FIG. 12(b)



(H-H CROSS-SECTION)

FIG. 13

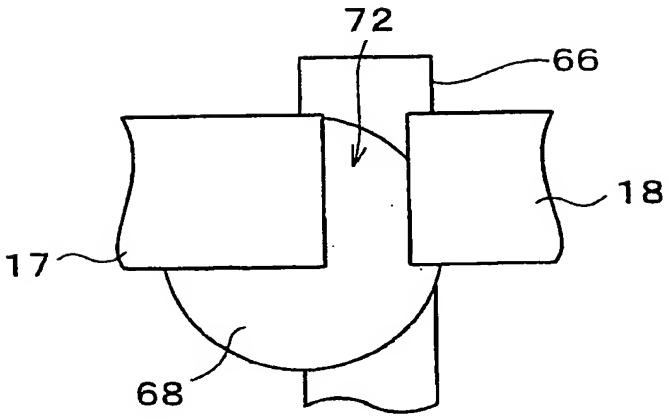


FIG. 14(a)

(CHANNEL SECTION PROCESSING IS COMPLETED)

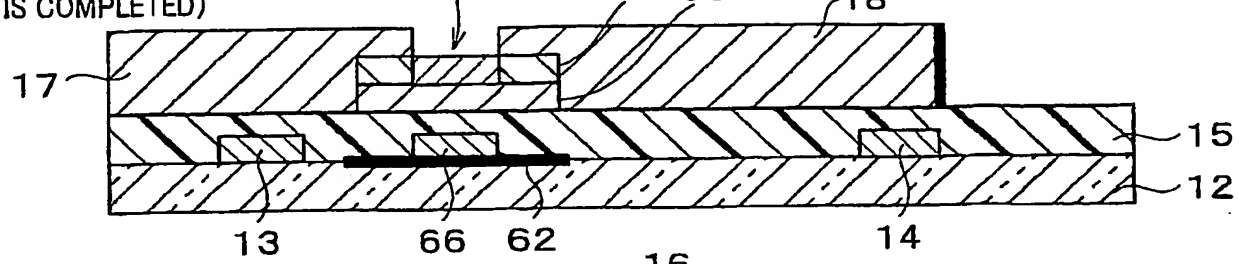


FIG. 14(b)

(LIGHT BLOCKING FILM IS APPLIED)

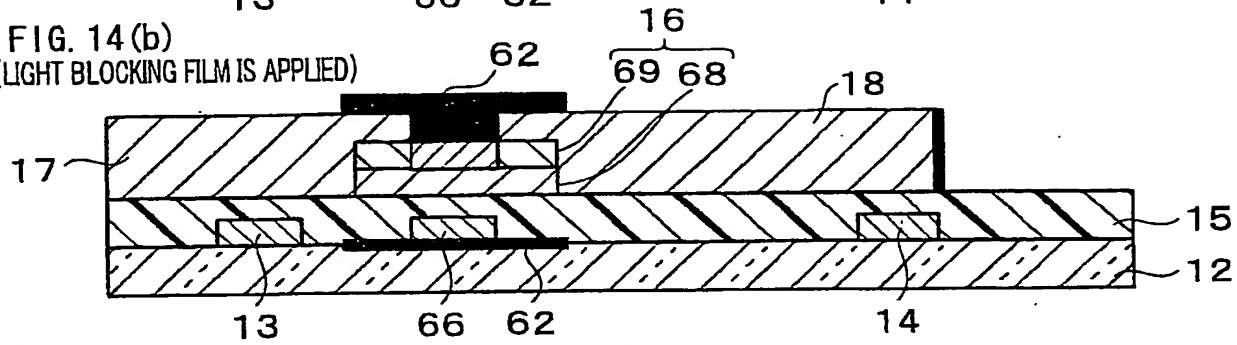
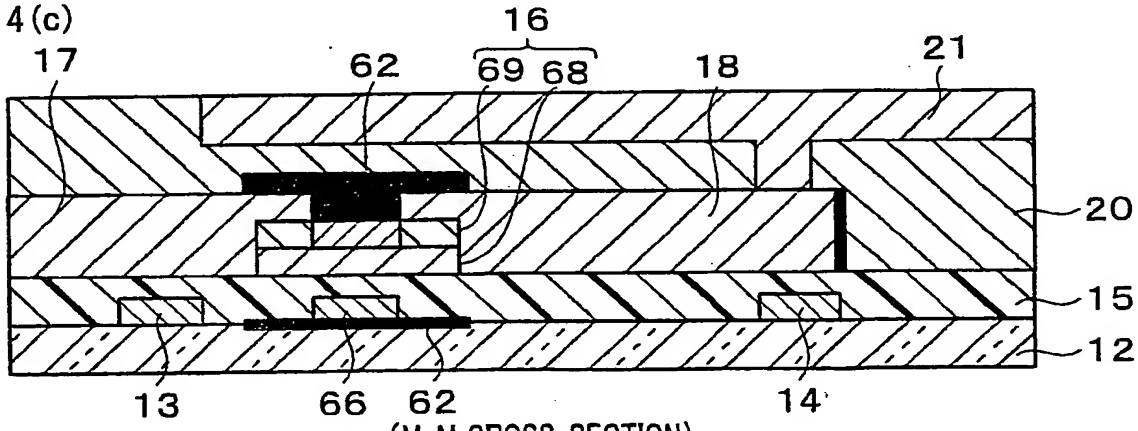


FIG. 14(c)



(M-M CROSS-SECTION)

FIG. 14(d)

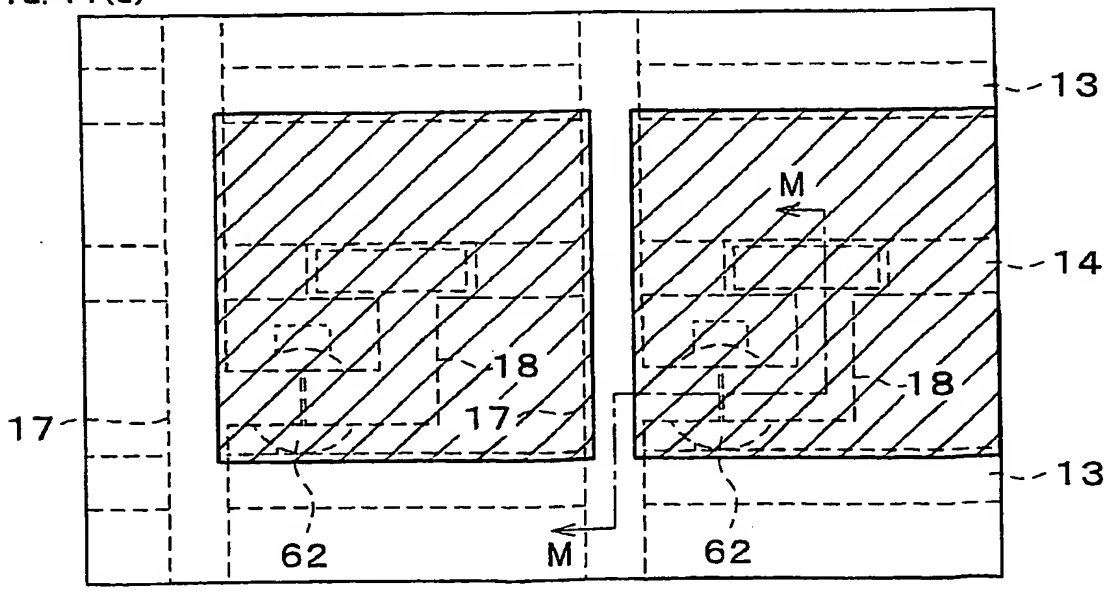


FIG. 15(a)

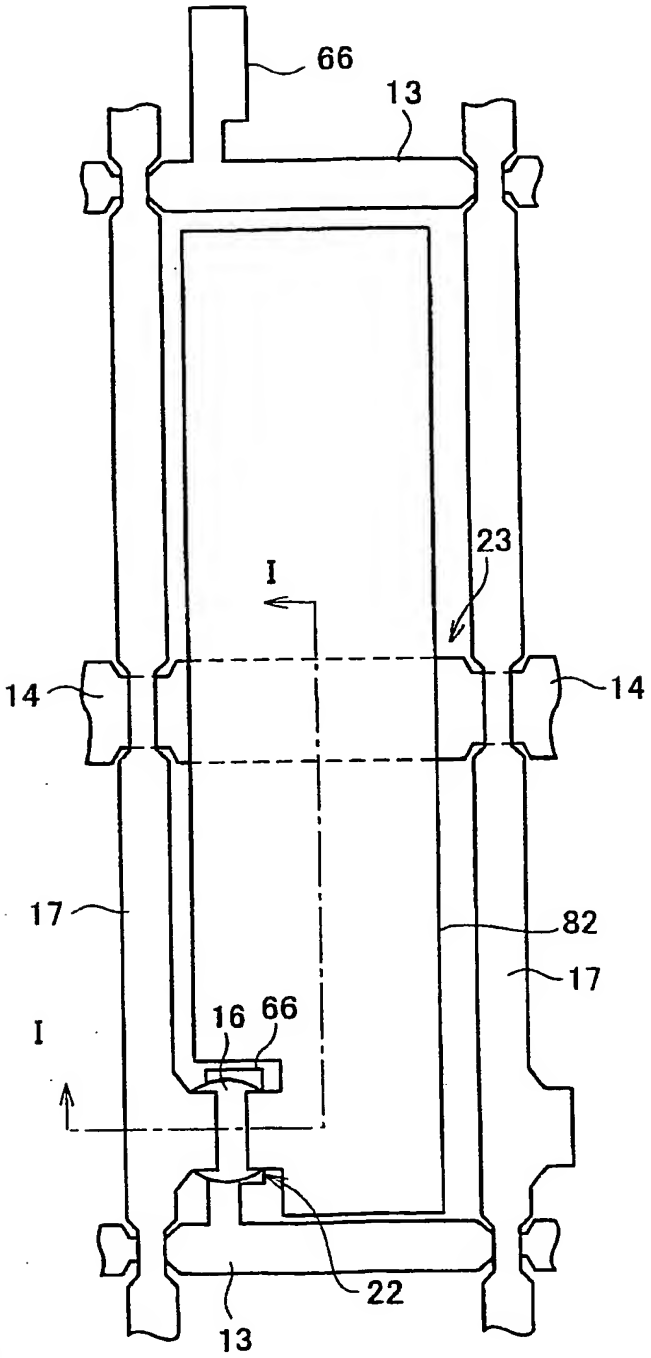
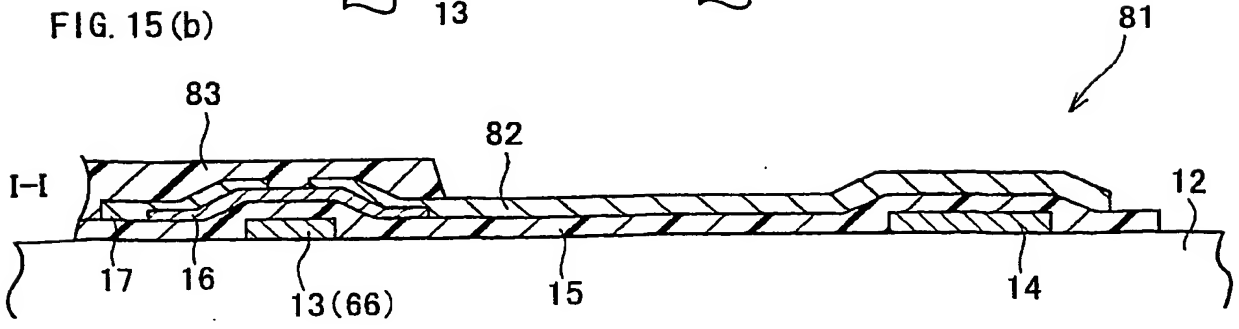


FIG. 15(b)



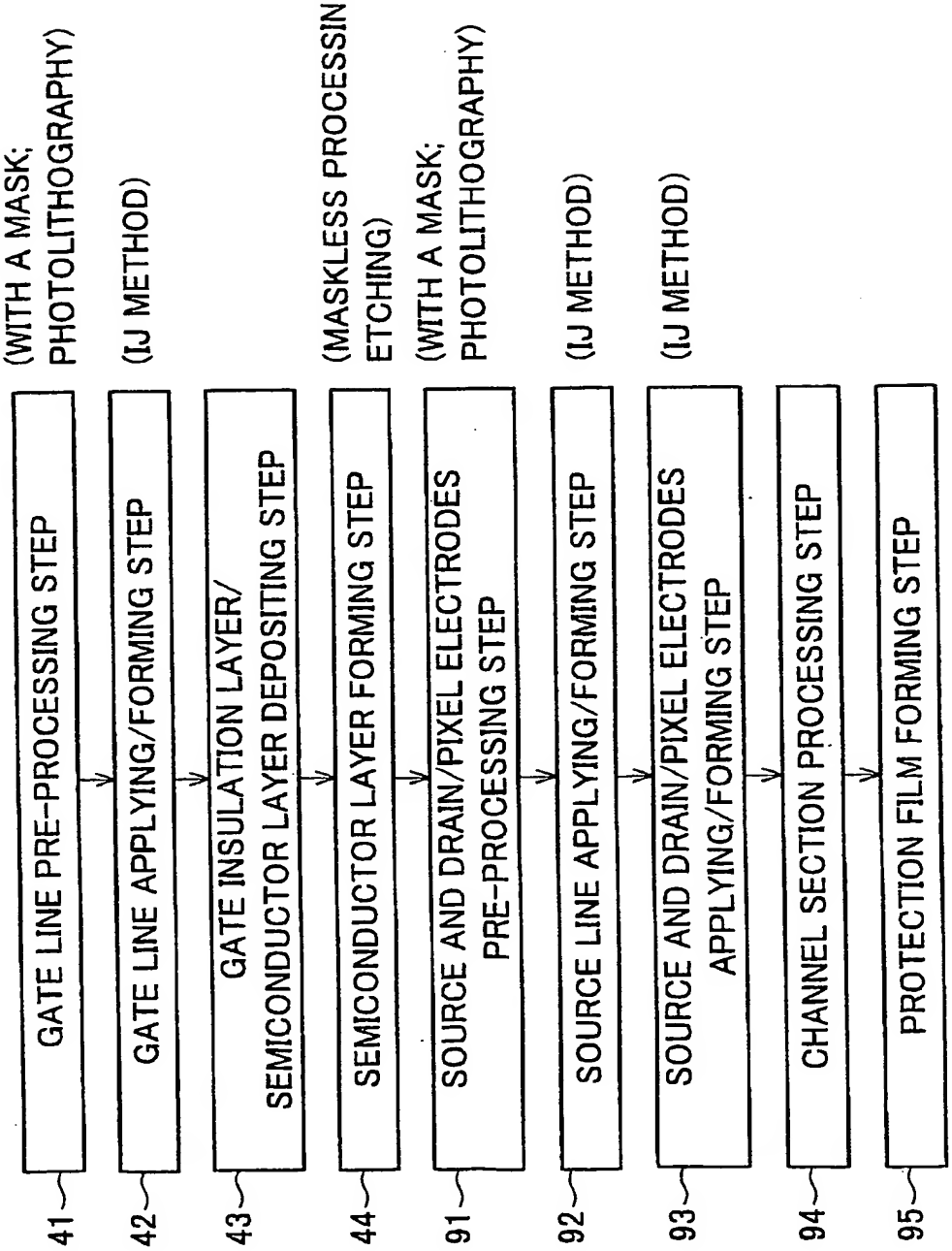

41
GATE LINE PRE-PROCESSING STEP
(WITH A MASK; PHOTOLITHOGRAPHY)
42
GATE LINE APPLYING/FORMING STEP
(IJ METHOD)
43
GATE INSULATION LAYER/ SEMICONDUCTOR LAYER DEPOSITING STEP
44
SEMICONDUCTOR LAYER FORMING STEP
(MASKLESS PROCESSING; ETCHING)
91
SOURCE AND DRAIN/PIXEL ELECTRODES PRE-PROCESSING STEP
(WITH A MASK; PHOTOLITHOGRAPHY)
92
SOURCE LINE APPLYING/FORMING STEP
(IJ METHOD)
93
SOURCE AND DRAIN/PIXEL ELECTRODES APPLYING/FORMING STEP
(IJ METHOD)
94
CHANNEL SECTION PROCESSING STEP
95
PROTECTION FILM FORMING STEP

FIG. 16

FIG. 17

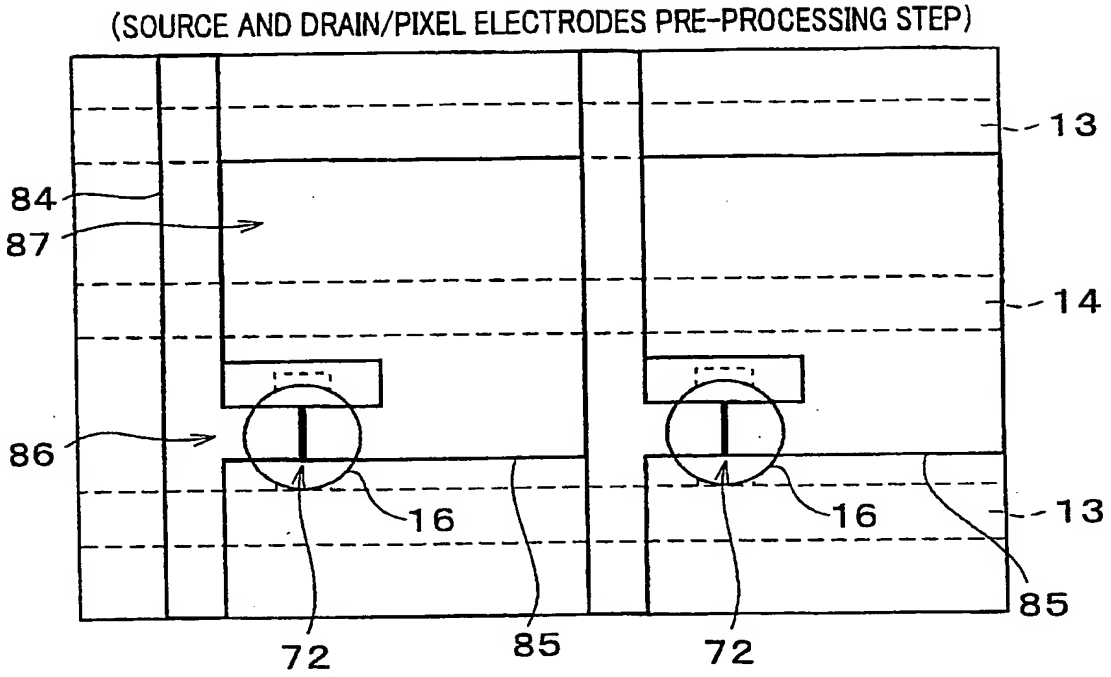

(SOURCE AND DRAIN/PIXEL ELECTRODES PRE-PROCESSING STEP)
13
84
87
14
86
16
16
13
85
72
85
72

FIG. 18(a)

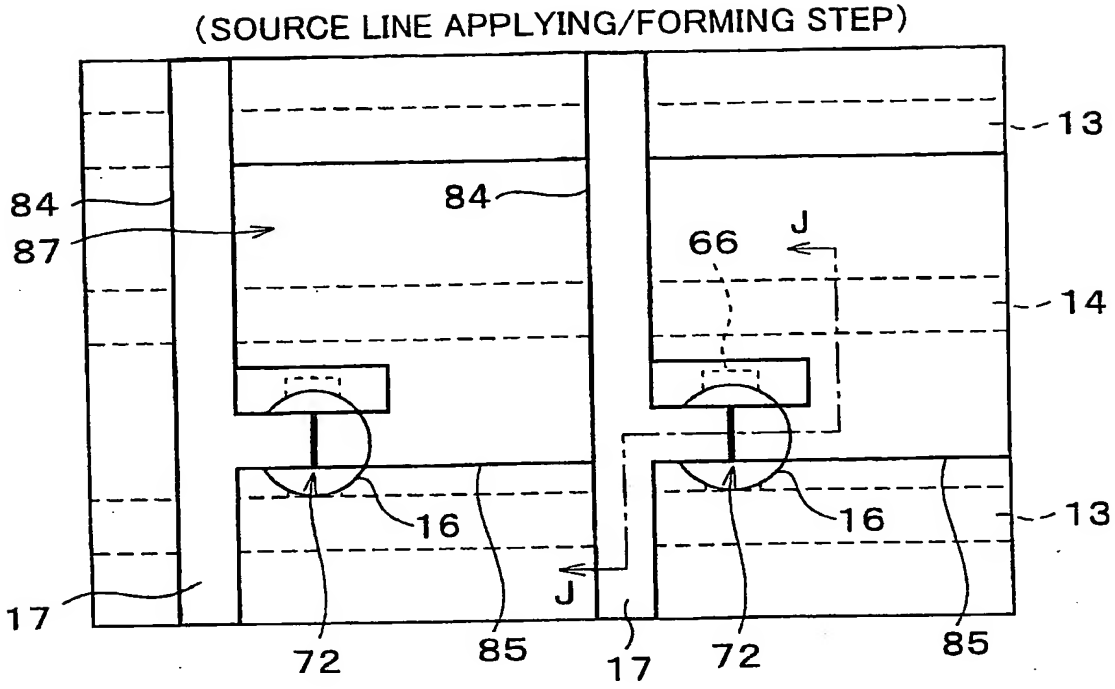


FIG. 18(b)

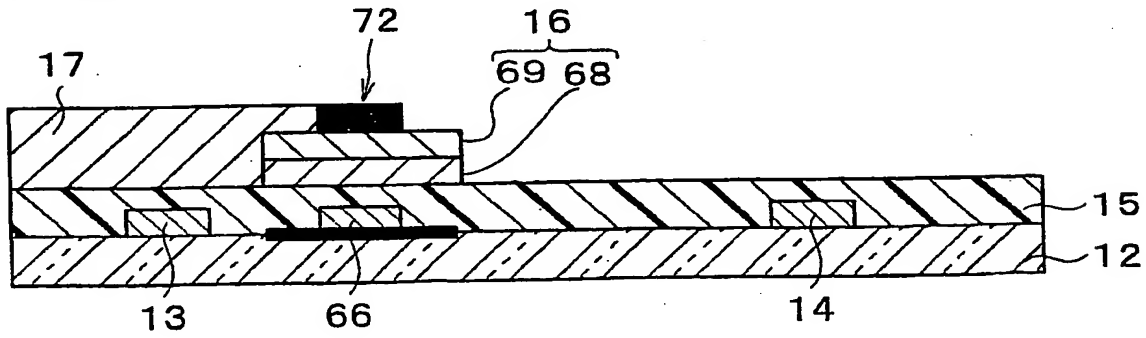


FIG. 19(a)

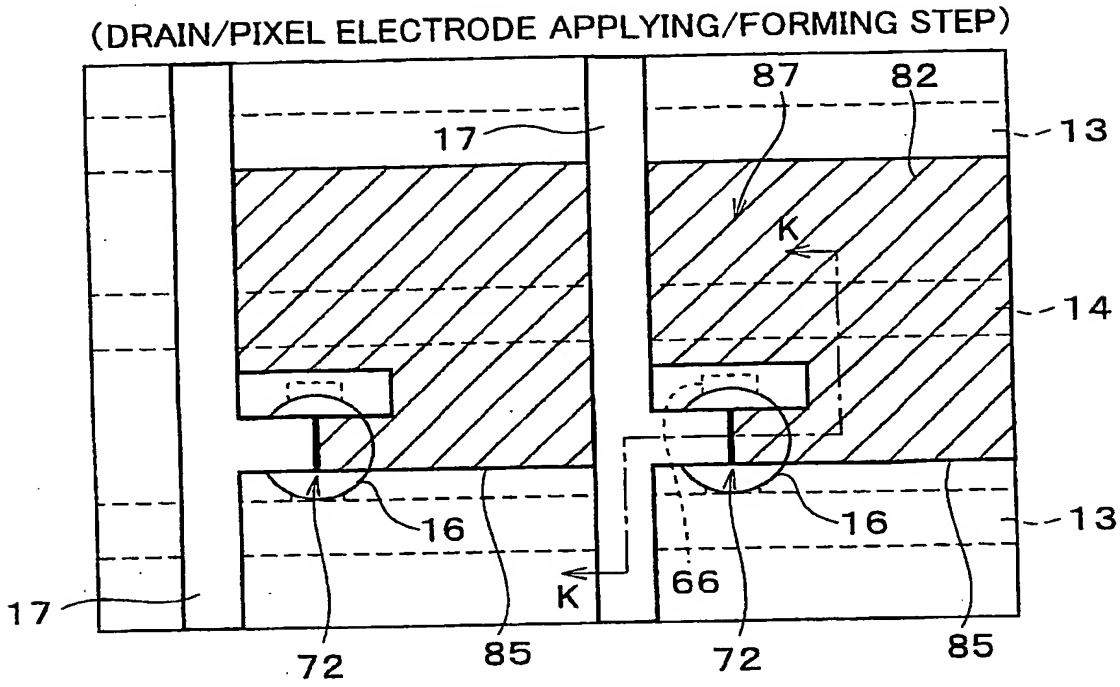


FIG. 19(b)

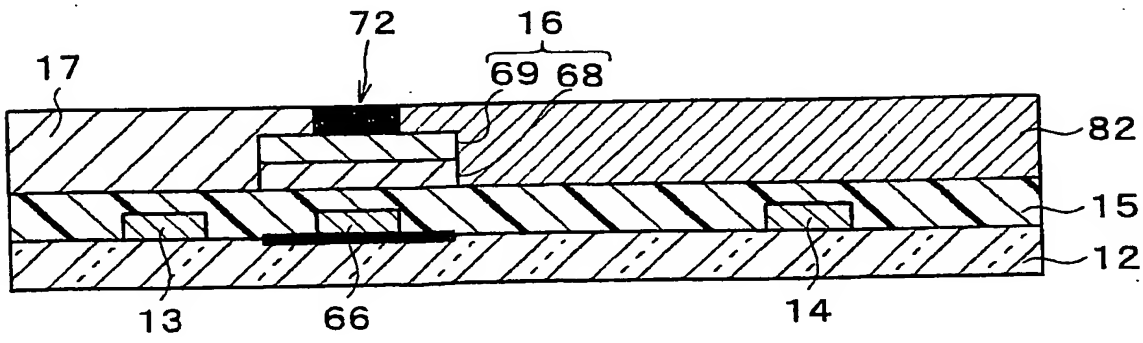


FIG. 20(a) (CHANNEL SECTION PROCESSING STEP)

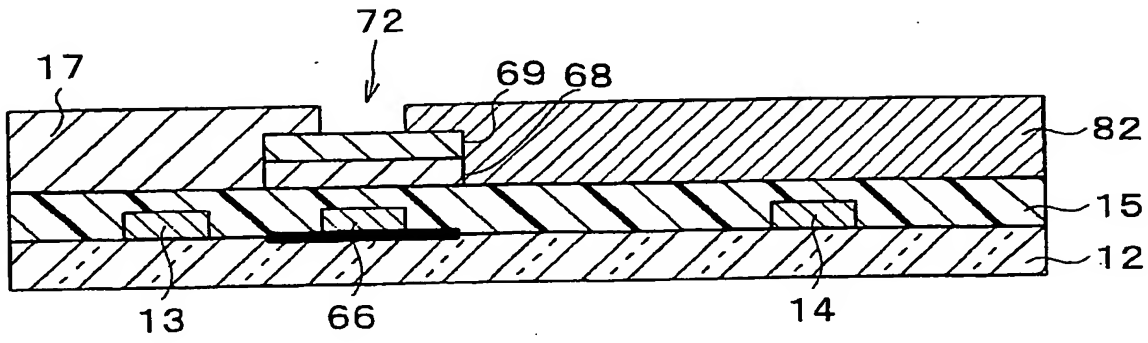


FIG. 20(b)

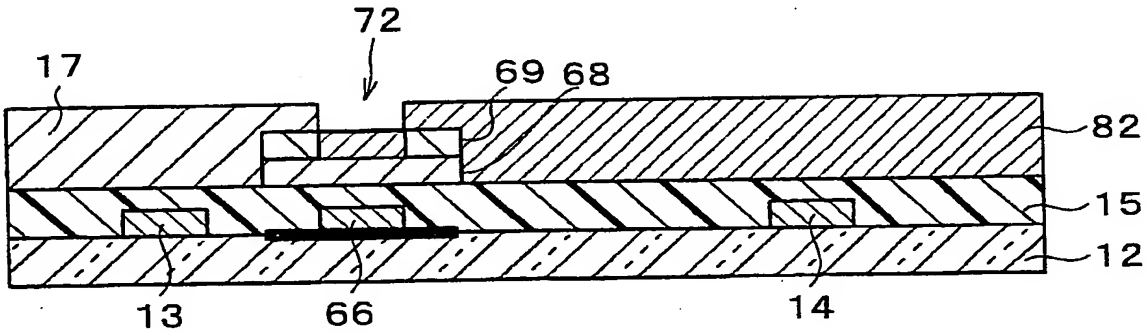


FIG. 21

(PROTECTION FILM FORMING STEP)

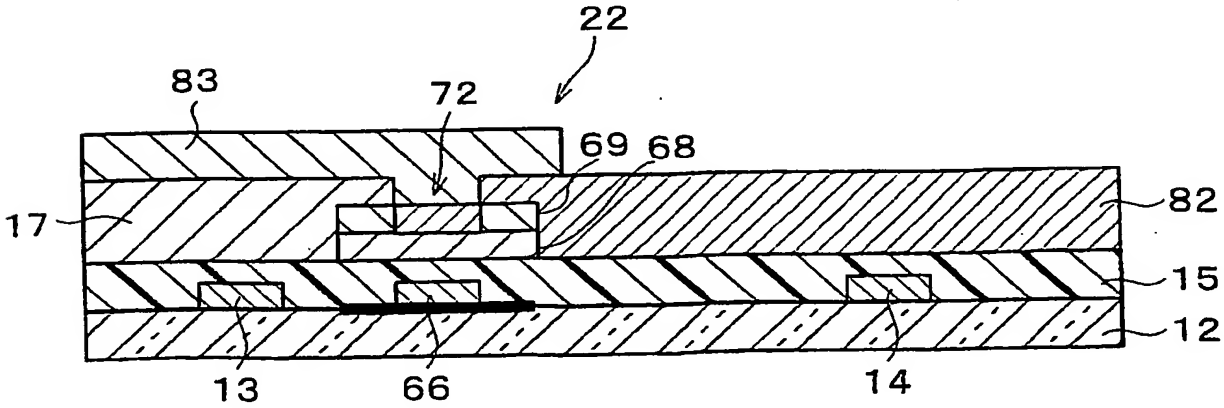


FIG. 22 (a)

(SEMICONDUCTOR LAYER FORMING STEP (DIRECT FORMING))

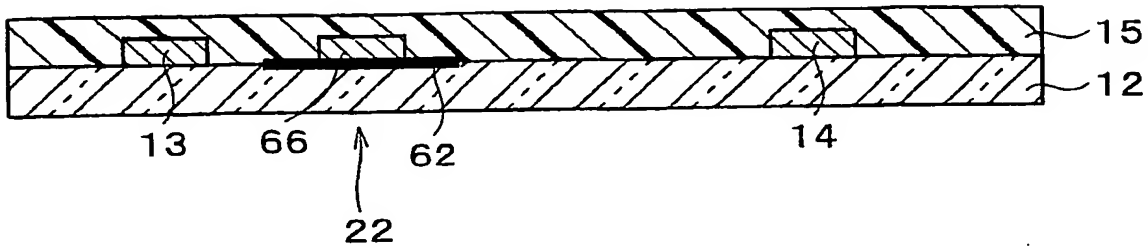


FIG. 22 (b)

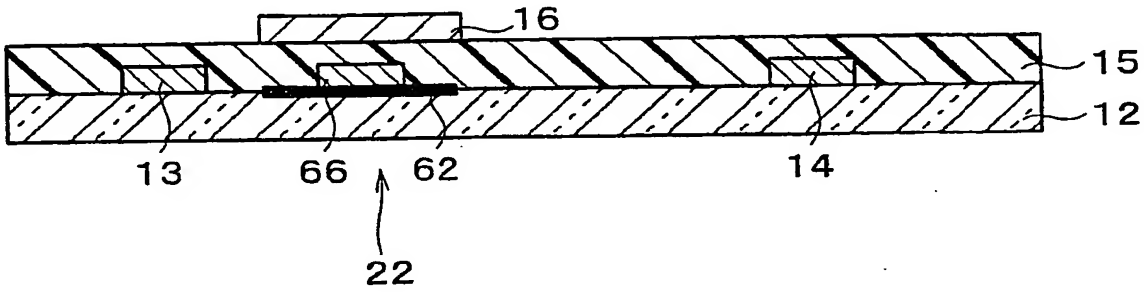


FIG. 22 (c)

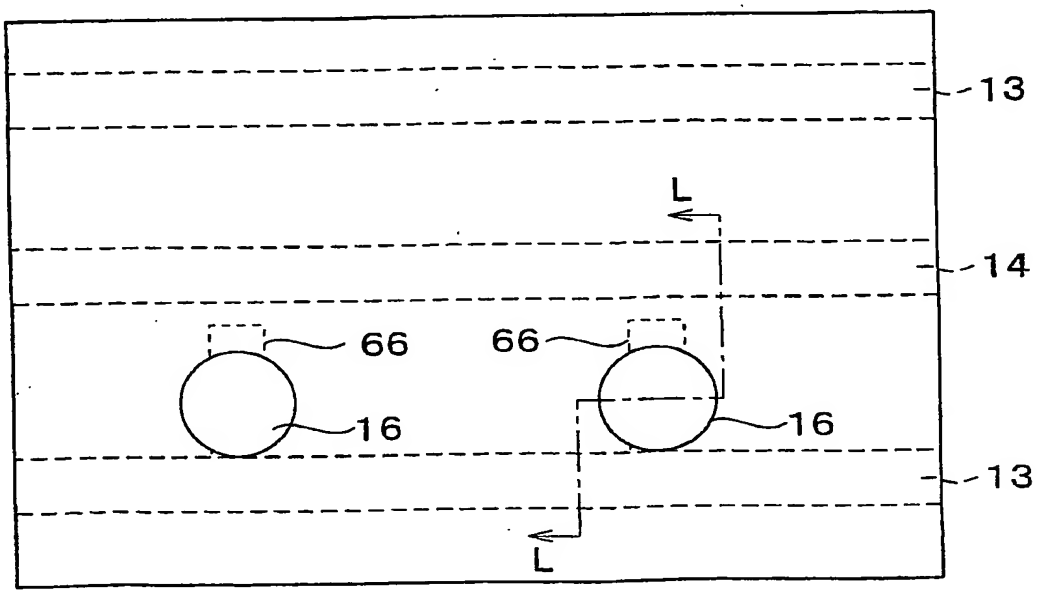


FIG. 23

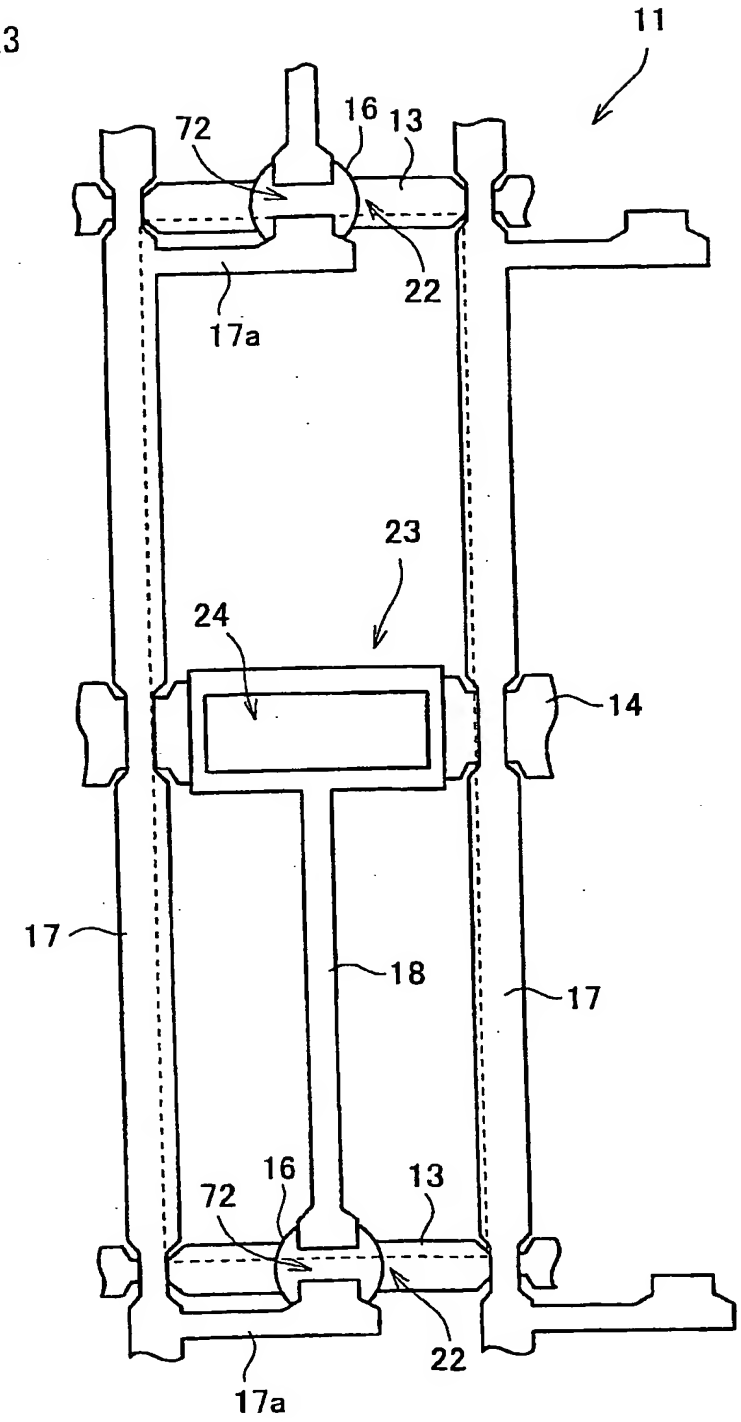


FIG. 24

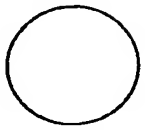


FIG. 25 (a)

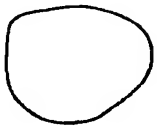


FIG. 25 (b)

FIG. 25 (c)

FIG. 26 (a)

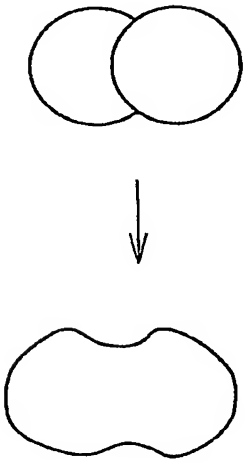


FIG. 26 (b)

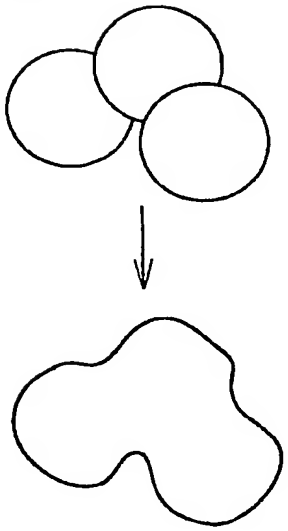


FIG. 27 (a)

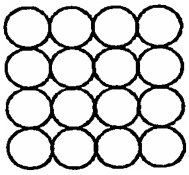
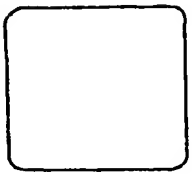


FIG. 27 (b)



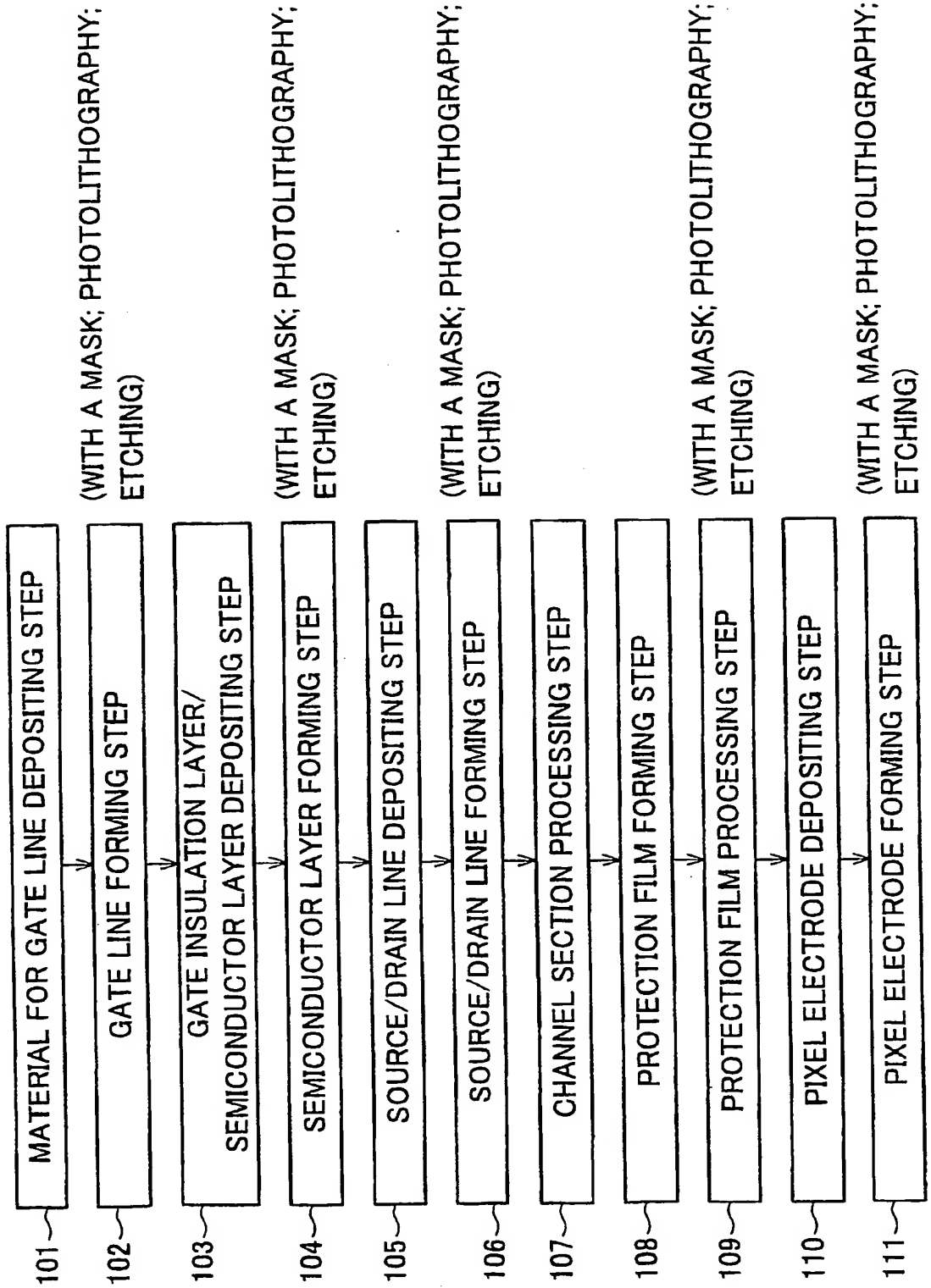

101
MATERIAL FOR GATE LINE DEPOSITING STEP
102
GATE LINE FORMING STEP
(WITH A MASK; PHOTOLITHOGRAPHY; ETCHING)
103
GATE INSULATION LAYER/ SEMICONDUCTOR LAYER DEPOSITING STEP
104
SEMICONDUCTOR LAYER FORMING STEP
(WITH A MASK; PHOTOLITHOGRAPHY; ETCHING)
105
SOURCE/DRAIN LINE DEPOSITING STEP
106
SOURCE/DRAIN LINE FORMING STEP
(WITH A MASK; PHOTOLITHOGRAPHY; ETCHING)
107
CHANNEL SECTION PROCESSING STEP
108
PROTECTION FILM FORMING STEP
109
PROTECTION FILM PROCESSING STEP
(WITH A MASK; PHOTOLITHOGRAPHY; ETCHING)
110
PIXEL ELECTRODE DEPOSITING STEP
111
PIXEL ELECTRODE FORMING STEP
(WITH A MASK; PHOTOLITHOGRAPHY; ETCHING)

FIG. 28

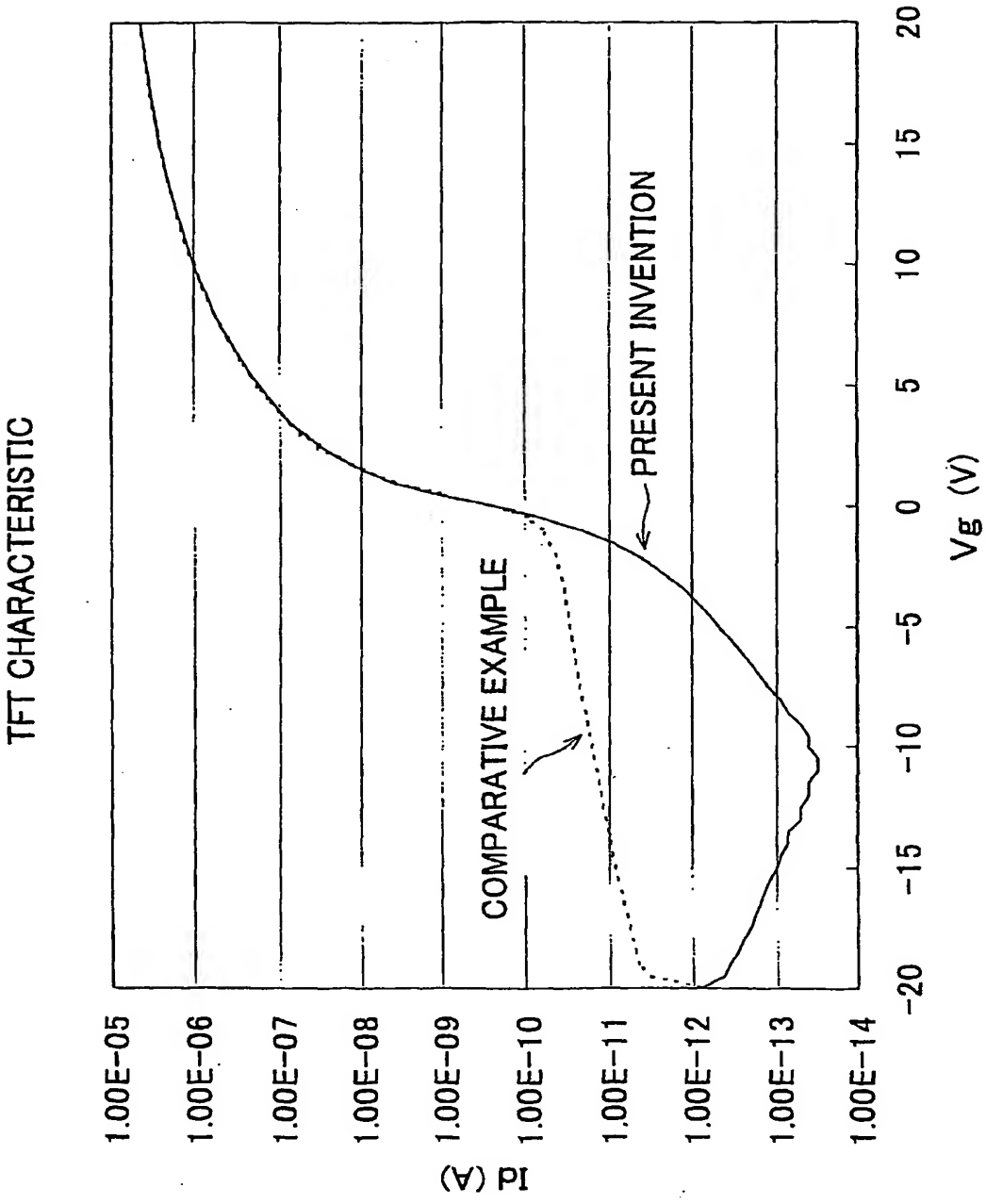

TFT CHARACTERISTIC
PRESENT INVENTION
COMPARATIVE EXAMPLE
Id (A)
1.00E-05
1.00E-06
1.00E-07
1.00E-08
1.00E-09
1.00E-10
1.00E-11
1.00E-12
1.00E-13
1.00E-14
Vg (V)
20
15
10
5
0
-5
-10
-15
-20

FIG. 29

FIG. 30

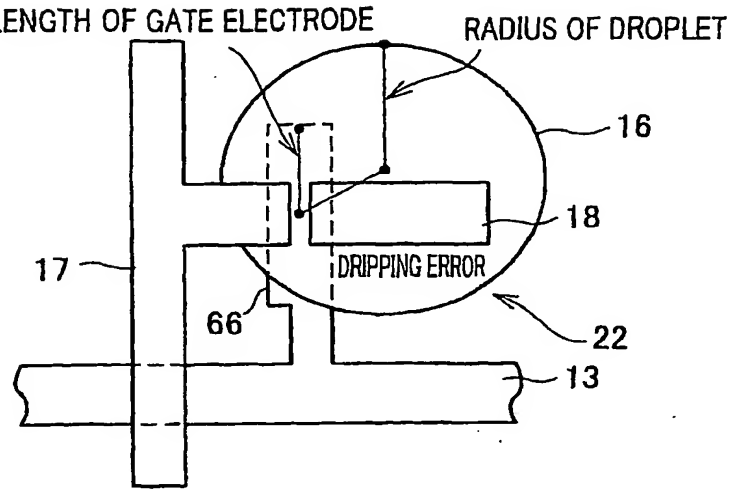


FIG. 31

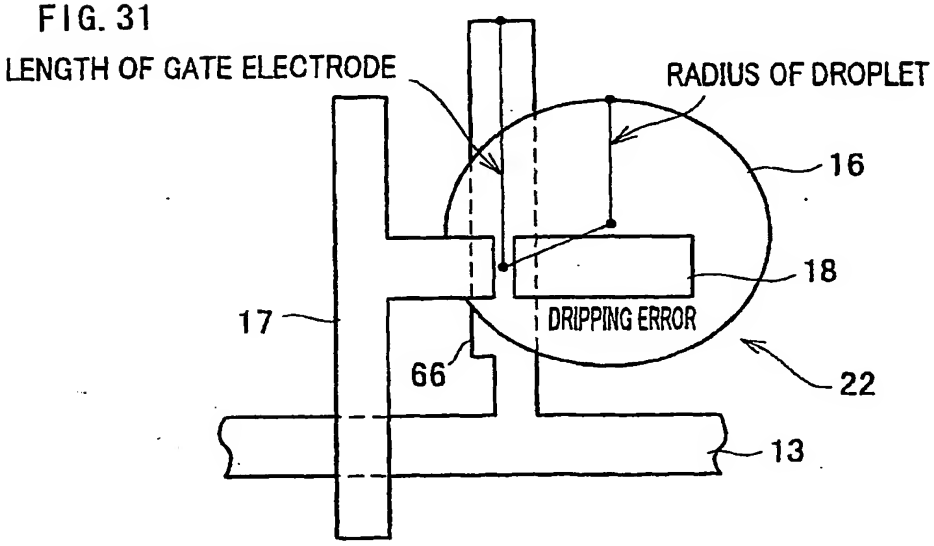


FIG. 32

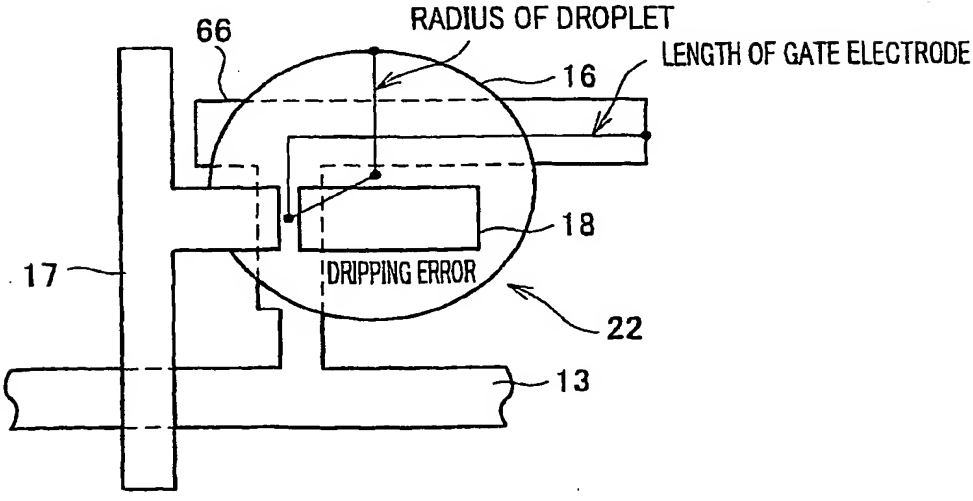


FIG. 33

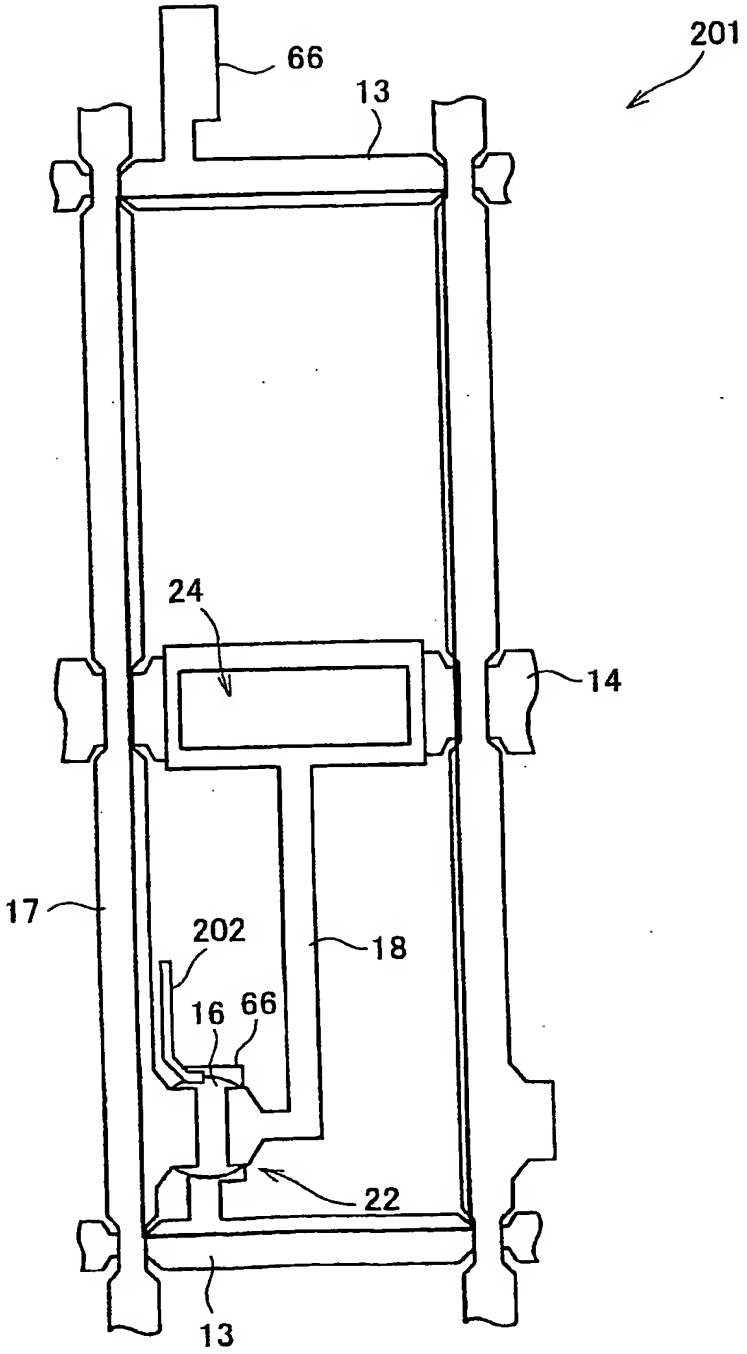


FIG. 34

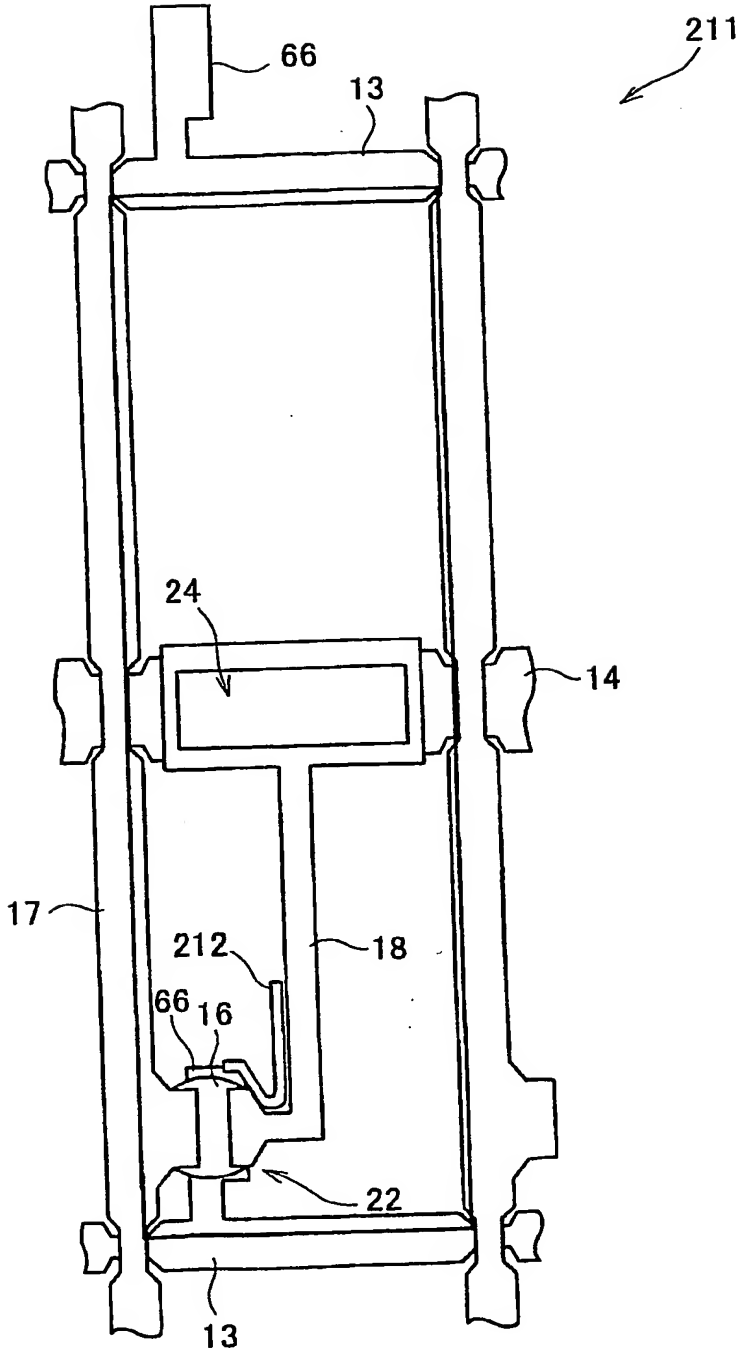


FIG. 35

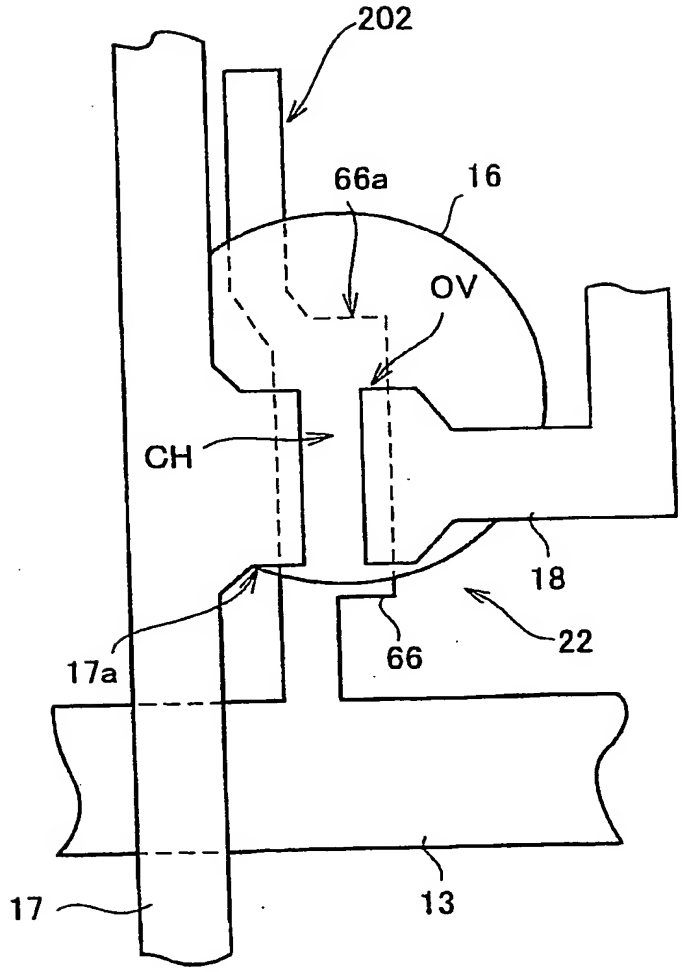


FIG. 36

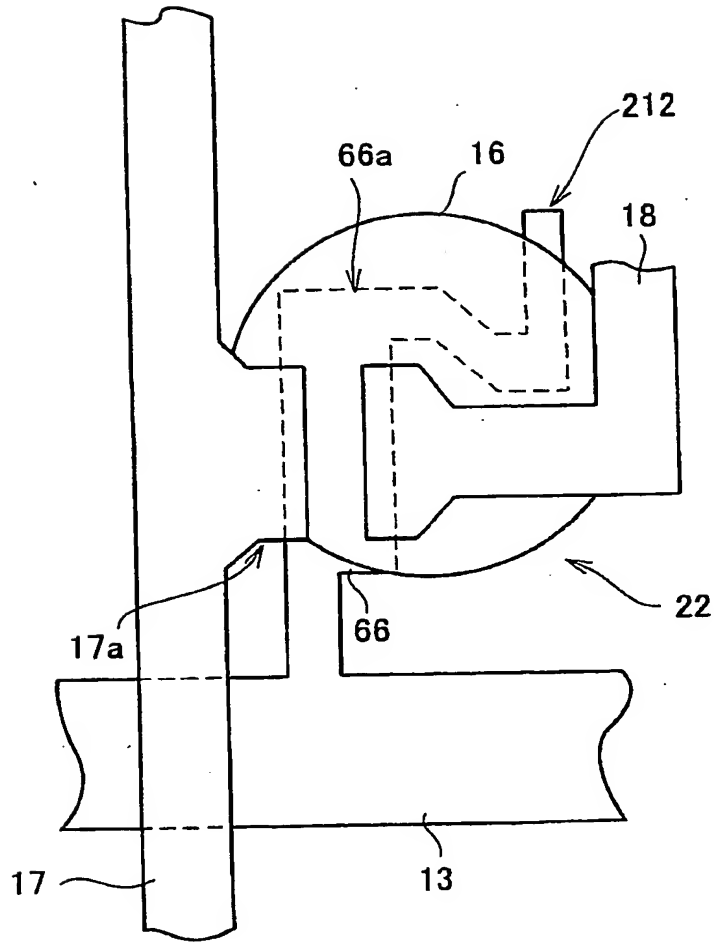
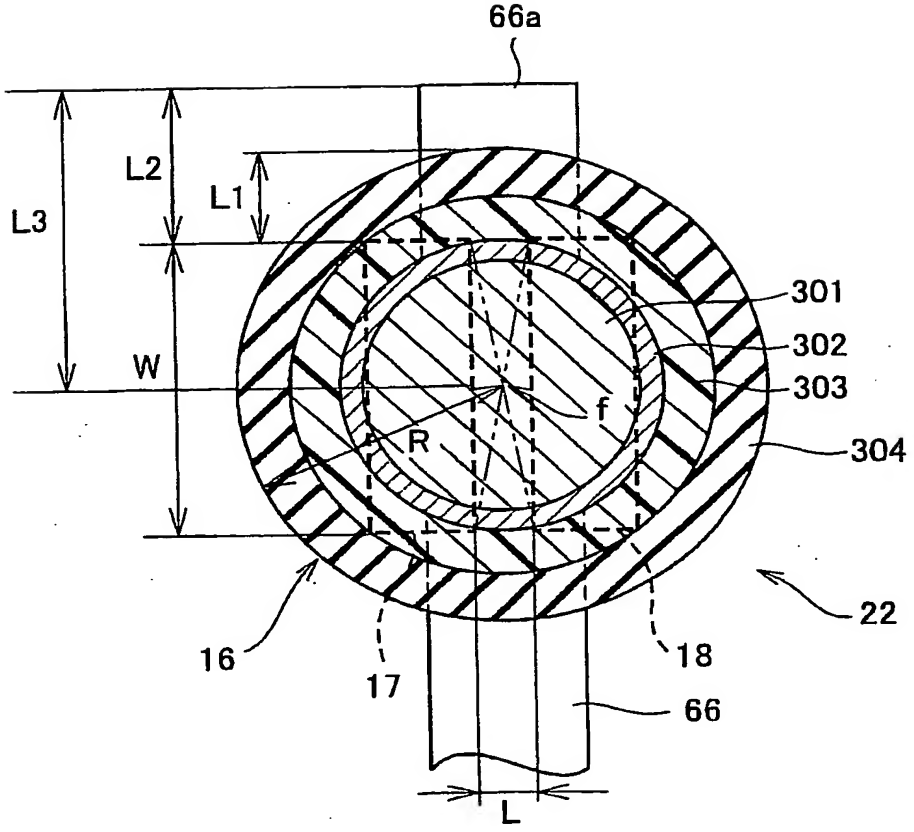


FIG. 37



$L1 > \Delta 1 + \Delta 2$

$L2 > \Delta 1 + 2\Delta 2$

$L3 > r + \Delta 1 + 2\Delta 2$

FIG. 38

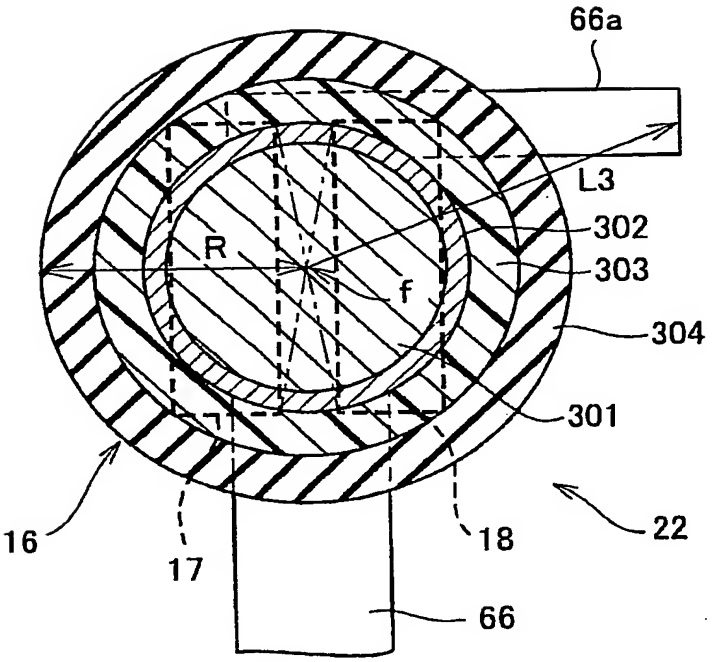


FIG. 39 (a)

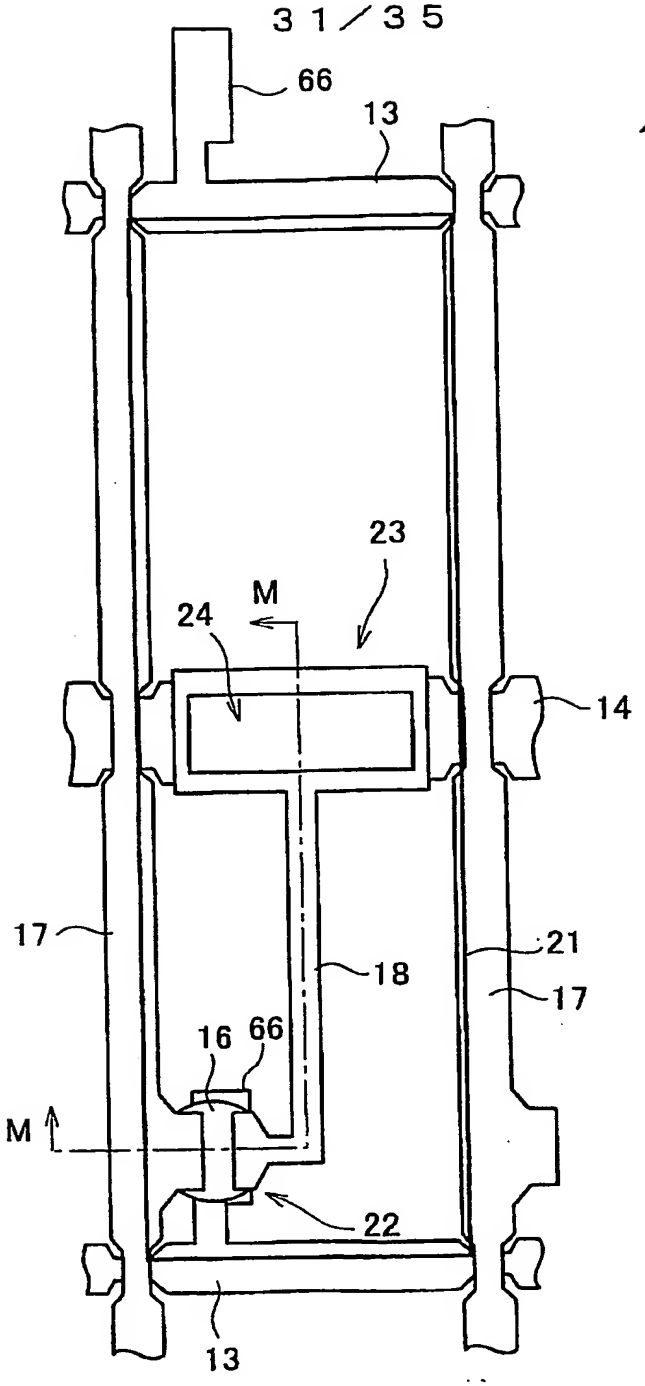
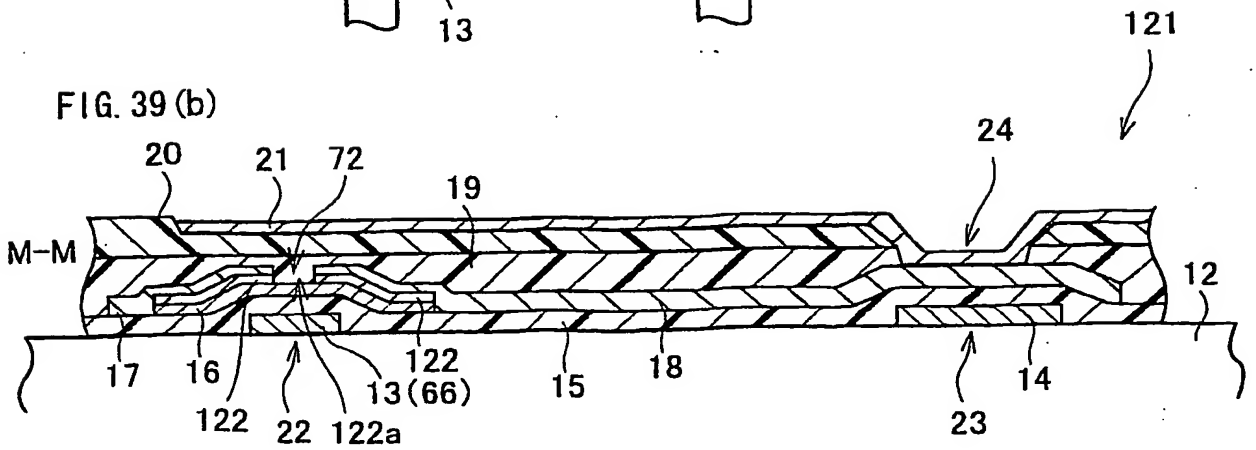


FIG. 39 (b)



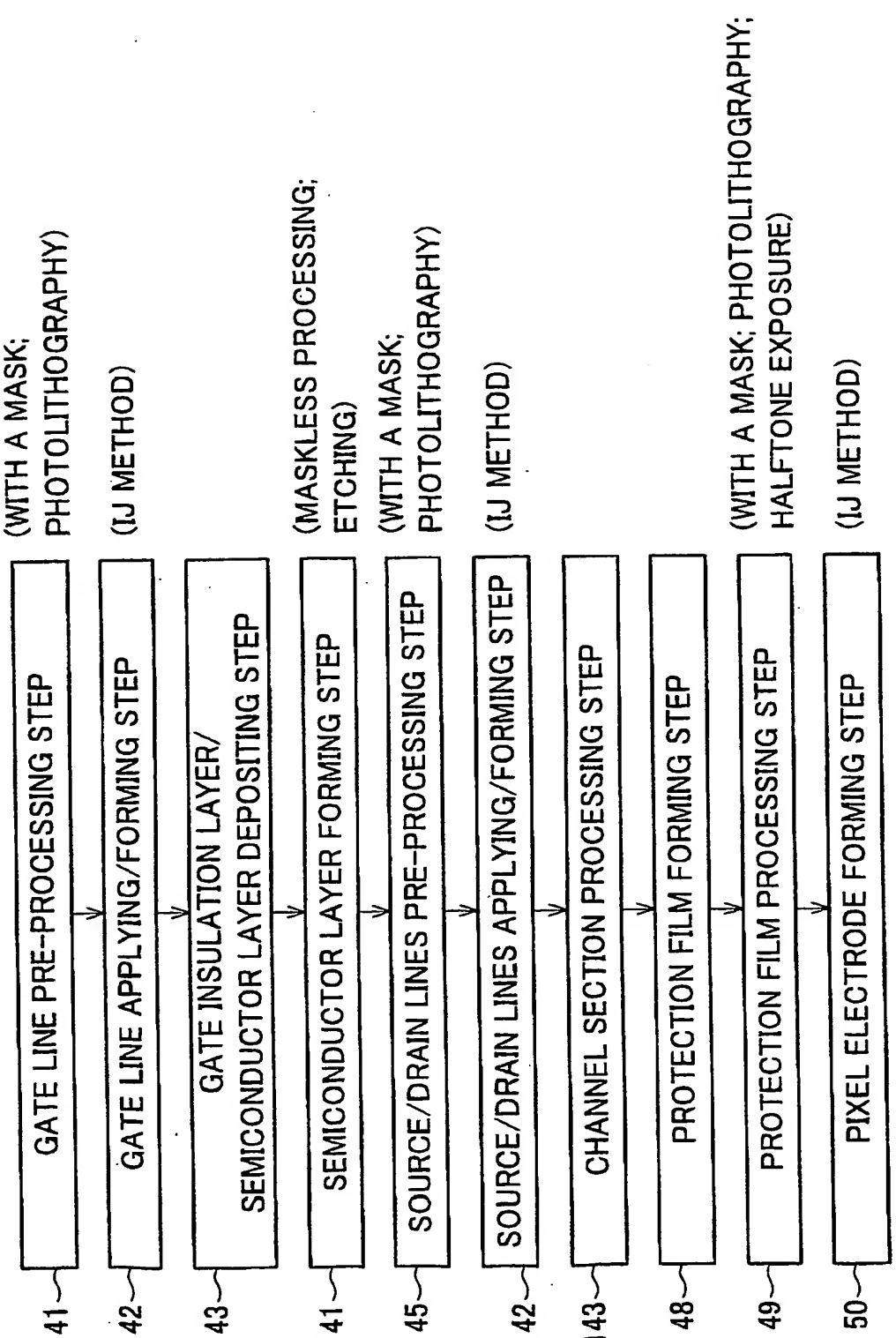

41
GATE LINE PRE-PROCESSING STEP
(WITH A MASK; PHOTOLITHOGRAPHY)
42
GATE LINE APPLYING/FORMING STEP
(IJ METHOD)
43
GATE INSULATION LAYER/ SEMICONDUCTOR LAYER DEPOSITING STEP
141
SEMICONDUCTOR LAYER FORMING STEP
(MASKLESS PROCESSING; ETCHING)
45
SOURCE/DRAIN LINES PRE-PROCESSING STEP
(WITH A MASK; PHOTOLITHOGRAPHY)
142
SOURCE/DRAIN LINES APPLYING/FORMING STEP
(IJ METHOD)
143
CHANNEL SECTION PROCESSING STEP
48
PROTECTION FILM FORMING STEP
49
PROTECTION FILM PROCESSING STEP
(WITH A MASK; PHOTOLITHOGRAPHY; HALFTONE EXPOSURE)
50
PIXEL ELECTRODE FORMING STEP
(IJ METHOD)

FIG. 40

FIG. 41 (a) (SEMICONDUCTOR FORMING STEP)

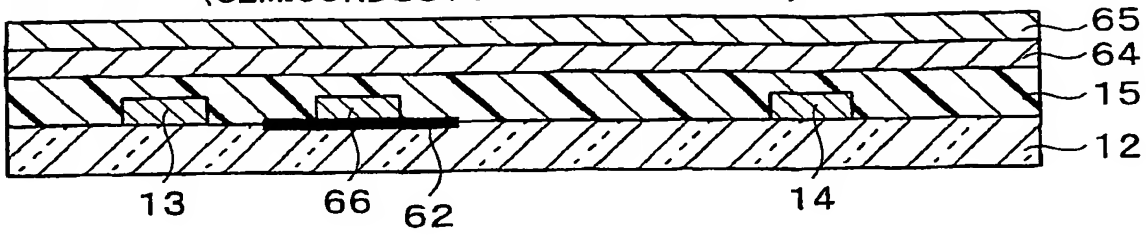


FIG. 41 (b)

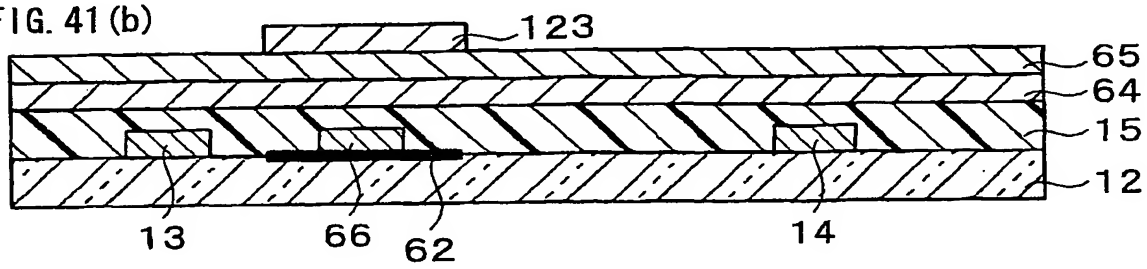
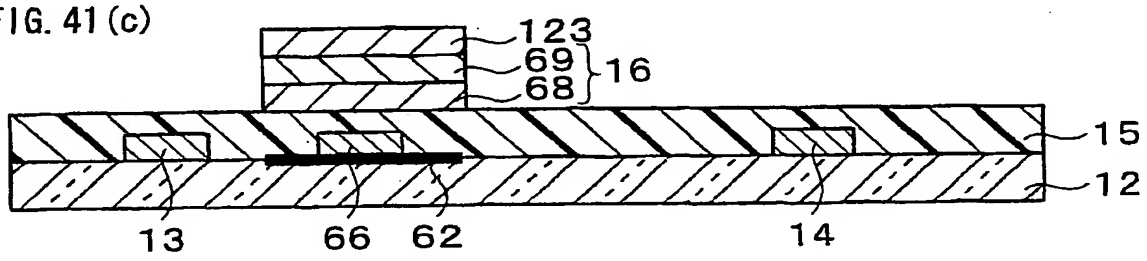


FIG. 41 (c)



(N-N CROSS-SECTION)

FIG. 41 (d)

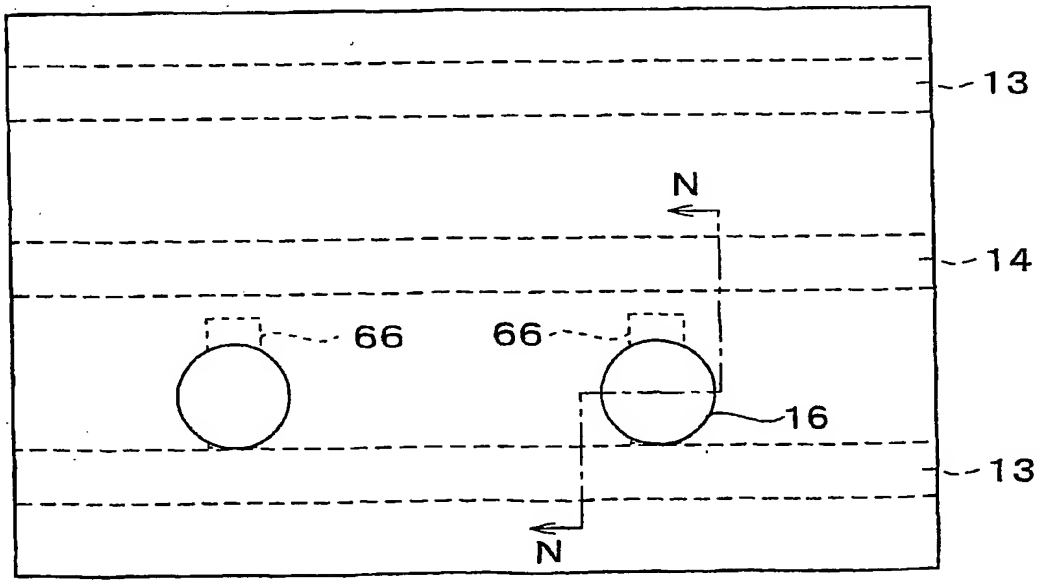


FIG. 42(a) (SOURCE/DRAIN LINE PRE-PROCESSING STEP)

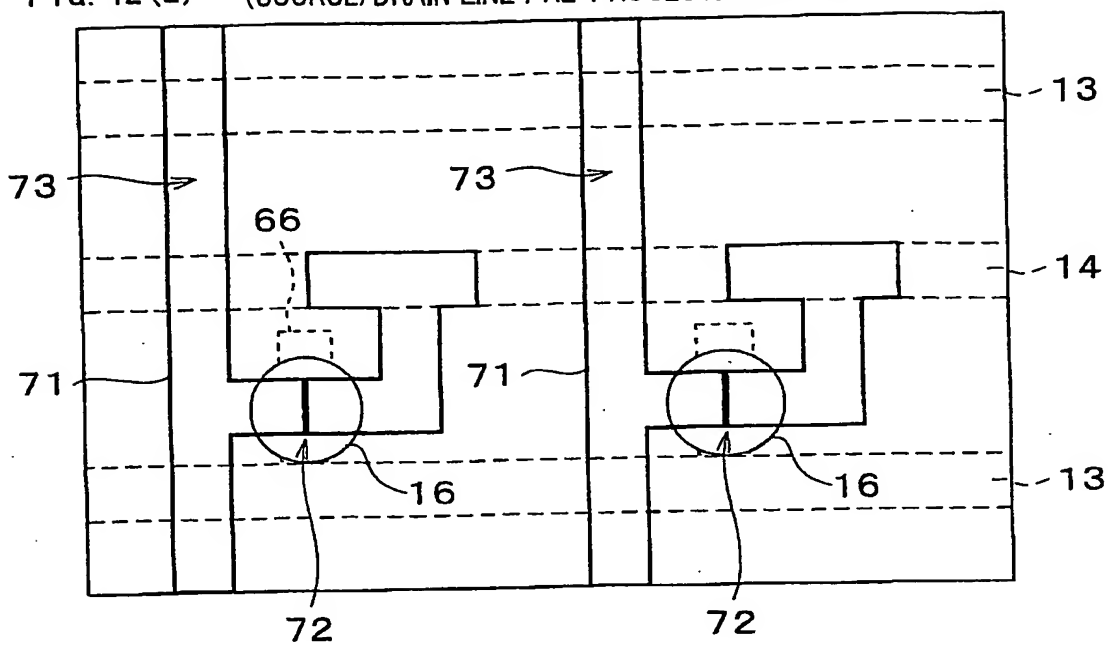


FIG. 42(b) (SOURCE/DRAIN LINE FORMING STEP)

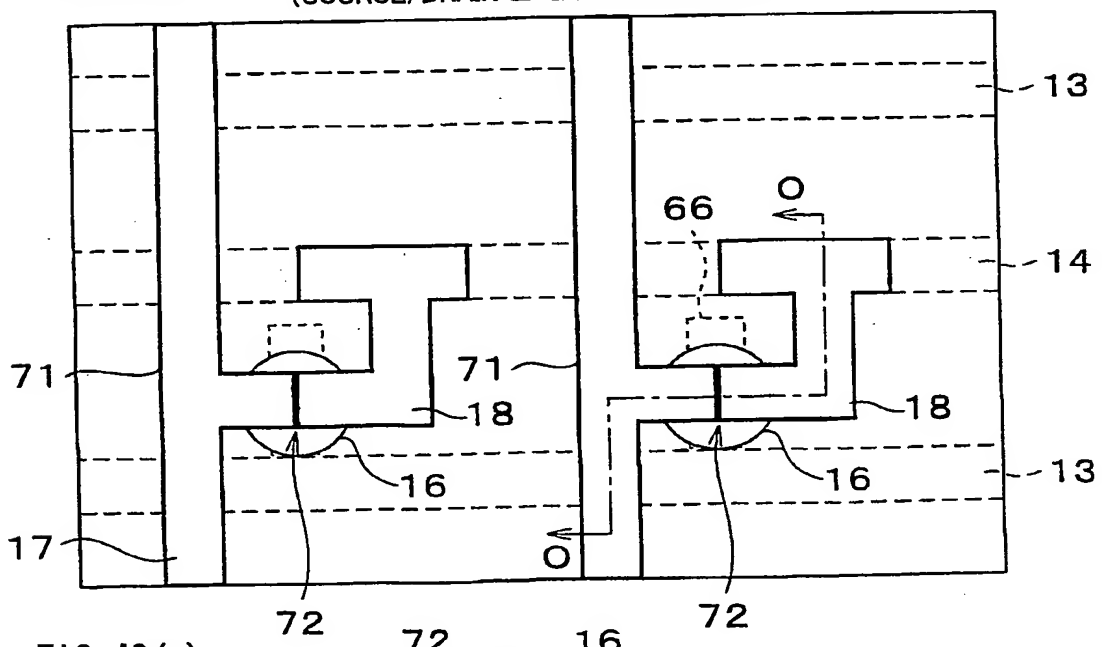
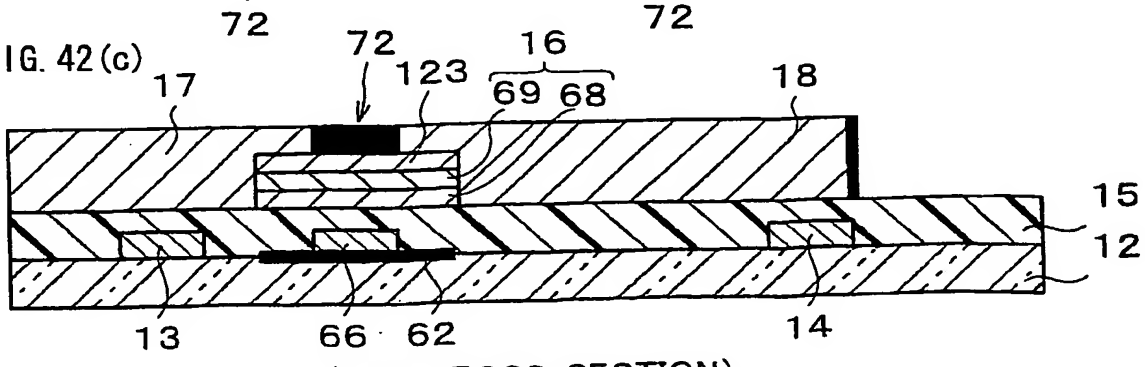


FIG. 42(c)



(O-O CROSS-SECTION)

FIG. 43(a)

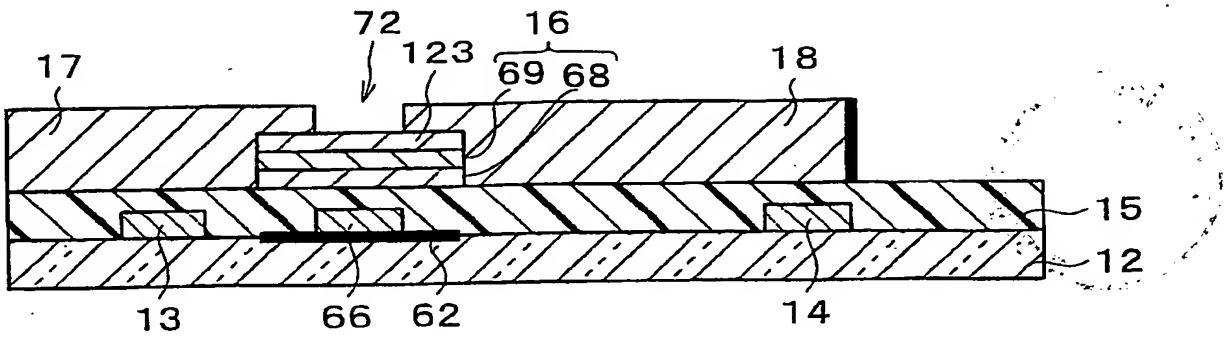


FIG. 43(b)

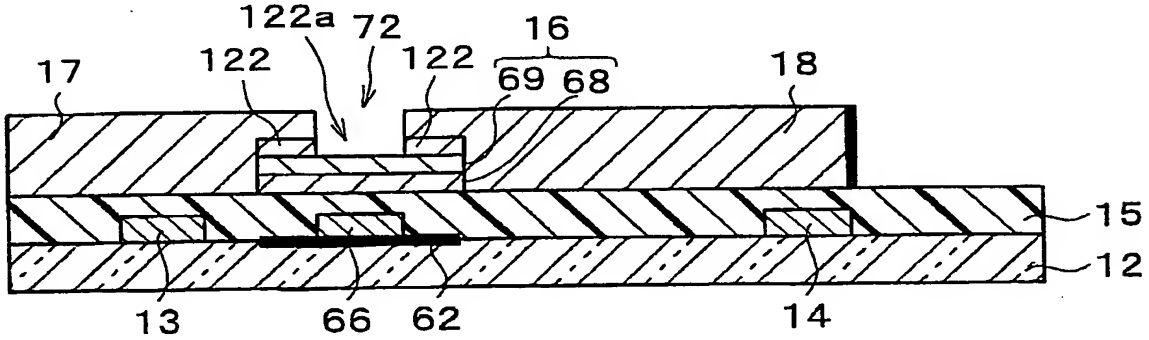


FIG. 43(c)